

QUALIFYING A PROCESS TO J-STD-001B

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Introduction

Electronics manufacturers are faced with the difficult task of proving that a candidate manufacturing process can produce acceptable hardware, either to the customer of the product, or for internal quality control. In the past, assembly level specifications (e.g. MIL-STD-2000A) told you exactly how to go about such a demonstration. It wasn't always precisely the optimum, but you didn't have to figure out all of the fine points of the qualification on your own. In our modern era, "how-to" specifications are now evil things and taboo to all involved with them. The users now have to determine many of the process qualification steps on their own, and sadly, many don't have the faintest idea where to start. This paper addresses some of the fundamentals that have to be considered when qualifying a candidate process to the B revision of J-STD-001.

MIL-STD-2000A

No discussion about process qualifications would be complete without briefly touching the venerable MIL-STD-2000A. This was one of the first documents that went about process qualification. A question that is asked frequently by military manufacturers is "What testing do I do now that MIL-STD-2000A has been canceled without replacement?" The answer is MIL-STD-2000A, Appendices A and C, unless told otherwise by your contract officer. My specialty is not contractual law, but my understanding is that the day you signed the contract, the revision in place at that time is the revision you manufacture to. Any changes that come later are immaterial unless the contract is upgraded to the new revision. If you still manufacture to MIL-STD-2000A and the contracts have not been changed, then you still have to do Appendix A and C testing if you want to use a new process. There are many manufacturers who are going through this process even today because from a contractual standpoint, it is the path of least resistance. A great deal more information on this topic can be found in IPC-TP-1090.

J-STD-001, Revision A

J-STD-001, Revision A was developed about the same time as MIL-STD-2000B. MIL-STD-2000B died a political death in Washington, but the two documents were very similar. With the exception of a few commas, the process qualification protocol in J1A was identical to that proposed for MIL-STD-2000B, and has been used as an acceptable protocol since J1A was implemented (January 1995). IPC-TP-1090 also discusses J1A process qualification. The salient points to take from the J1A process qualification are as follows:

- Appendix D (SIR) and Appendix F (Ionics) are the qualification protocols
- Test Substrate: IPC-B-36 standard test assembly (others possible but seldom used)
- Metalization: bare copper, no OSPs
- Solder Mask: minimal solder mask only as LCC standoff (bumps)
- Starting cleanliness: Precleaned to less than 1 ug NaCl equivalence per square inch

- Components: Four 68 I/O LCCs on each test board (5 mil standoff)
- Number of SIR test patterns: 10 SIR patterns per board
- Sample Size: 3 unprocessed controls, 3 candidate process for both SIR and Ionics
- Coating: None
- Ionics: Automated ionic cleanliness testers
- Ionics Pass / Fail: Historical 10 ug/in² NaCl equivalence
- SIR: Seven days at 85C/85% RH, 50 volt bias, 100 volt measure (method 2.6.3.3A)
- SIR Pass / Fail: 100 megohms on all patterns, measured at 96 and 168 hours, 500 megohms at the final ambient reading, no corrosion or metal migration.

If your candidate process had ROSE values less than 10 ug NaCl equivalence per square inch (adjusted to machine type), and the candidate boards passed the requirements of the SIR testing, then you could use the new manufacturing process on your product. J1A represented a somewhat improved (depending on who you talk to) method of examining a candidate process and determining some level of minimum performance.

A frequently asked question has been “if I qualified to the A revision (J1A), must I do the more complex testing of J1B?”. The answer is no, there is a grandfather clause. See the note in J-STD-001B, paragraph 4.2. Of course, your customers can always force you to redo the testing.

Philosophy Change - J1A to J1B

J1B took a radically different approach to specifications. For many years, specifications dictated exactly how something was done. Choices were very limited and the resultant data was not open to much interpretation. Many people have this concept ingrained into them. With the DoD move away from “how-to” specifications to performance based specifications, a manufacturer now has a greater freedom or flexibility, but now has to figure out many of the background issues. Many companies are struggling with the concept.

IPC-TR-467, published by Jim Maguire, Boeing, and myself, details some of the rationale for the approaches taken in J1B, Appendix D. There is a complete change in philosophy between J1A and J1B. In J1A, we took a precleaned standard substrate, so we had no outside effects, processed the substrate through our reflow operations, and tested it. This was fine, as far as it went. Many manufacturers were able to discriminate between good and bad processes doing so? But inevitably, the questions were raised:

- The B-36 board is nothing like my product. How applicable is the test data?
- I have my own internal test vehicle. Why can't I use that?
- The B-36 has very little solder mask and bare copper metal. It is nothing like my SMOBC boards with HASLed tin-lead. Why use it?
- The B-36 is pre-cleaned. I don't preclean my bare boards. What about fabrication residues?
- What about interactions between different fluxes (HASL, paste, wave, touchup)?
- What about compatibility issues between cleaners and masks, fluxes and masks, etc.?
- I normally conformally coat my boards. Why don't I coat the B-36?
- My product functions in a condensing environment. Why do I test the coupon in a static (non-condensing) environment?

All very valid questions and deserving of answers. There is no perfect “one size fits all” test protocol. Having a standard substrate allows you to have a set pass/fail level and compare different processes, but there was often a wide gap between the substrate and the product it was supposedly representing. Having a tailored substrate allowed you to be much more representative of product, but the interpretation of data was open to engineering judgment and often subjective. With the Appendix D protocol in J1B, the best of both worlds was attempted.

J-STD-001B, Appendix D

Let us take a look at the salient points of J1B, Appendix D. A comparison to J1A levels is shown in Table 1.

- Appendix D is the only qualification protocol
- Test Substrate: Defaults to an IPC-B-36 standard test assembly, but alternative vehicles allowed and encouraged - must be representative of product
- Metalization: whatever is used on your product
- Solder Mask: whatever is used on your product, but the solder mask cannot cover SIR test patterns.
- Starting cleanliness: No precleaning. Test vehicle retains all residues from fabrication
- Components: Usually required, but depends on test vehicle
- Number of SIR test patterns: depends on the test vehicle
- Sample Size: 10 boards for each process combination
- Coating: if your product is coated, your test vehicle is coated.
- Ionics test: Recommended, but not required
- Ionics Pass / Fail (if used): 10 ug/in² NaCl equivalence as a default, can be specified otherwise
- SIR profile: to be chosen by manufacturer as most representative of product
- SIR Pass / Fail: related back to equivalent patterns on the IPC-B-36 board, depends on data set means of minimum values and variability of data set.
 - no corrosion
 - no metal migration bridging more than 20% of the spacing
 - if testing coated product, no failures of the coating (adhesion loss, cracking, reversion, etc.).

The entire approach in J1B is that just as your product is the sum of the residues of your manufacturing operations, so should your test vehicle represent that sum of residues, and more importantly, the effects of sum of the residues. If you have the most tightly controlled no-clean assembly operation in the world, but your incoming boards are loaded with detrimental residues, it is highly likely that your products are in jeopardy. If you have a solder mask that is incompatible with one of your cleaning agents in a later operation, you have a problem. The J1B approach is designed to look for these “gotchas”.

Where To Start

The best place to start is to determine if you have to do the qualification testing outlined in Appendix D. Such testing is done:

- When your customer requires it. After all, your customer drives the bus, even if they don't have a road map and should not have a license.
- When your customer feels that the Appendix D testing is the only acceptable way to demonstrate the Materials Compatibility requirement of J-STD-001B, paragraph 3.4.
- If you are using a flux that is not contained in the following J-STD-004 designations: RO (L0 or L1), RE(L0 or L1), OR(L0 or L1). This requirement is found in J-STD-001B, paragraph 4.2.
- When you are making a change to a proven (qualified) process. How much of a change requires re-testing is up for debate.

The fine points of when to do testing could be a paper in itself; so we will proceed with the assumption that you will be doing the testing, for whatever reason.

The Fabricator

A major new element to process qualification is the introduction of the question of fabrication residues and their effects. A large assembler might logically ask "must I do the qualification testing for each of my 20 bare board suppliers?"; usually with a sinking feeling in the stomach. The answer is potentially yes and could therefore get very expensive. At this point, the assembler should be asking the following questions:

- Do I really need all those fabricators? Can I pare it down to a more reasonable value?
- How well do I know the incoming cleanliness condition of my bare boards?
- Have I ever looked at bare board cleanliness?
- Are there seasonal variations or lot-to-lot variations to the cleanliness of the bare boards?
- Have the traditional ionic cleanliness tests or Bellcore tests been sufficient to allow me to differentiate good from bad bare boards (residue-wise)?

Again, the answering of these questions could fill volumes, and could be approached in many different ways. It is highly recommended that you do testing of bare board cleanliness by ion chromatography per IPC-TM-650, method 2.3.28. This is a far better indicator of bare board cleanliness than any other method available. For bare board cleanliness tests, you can use actual product.

Let us proceed with the assumption that you know the cleanliness levels of your bare boards and have chosen your "worst case" fabricator. Most process evaluation methods are similar in that if you look at the worst case situation and can pass the requirements, then it can be assumed that you will pass the less stringent cases as well.

The Test Vehicle

Now that you have chosen which fabricator(s) to use, you must select the test vehicle. The default test vehicle is the IPC-B-36 standard test assembly. The manufacturer must determine how representative the B-36 is of the actual product. In many cases, the B-36 is significantly different from actual product. There are other test vehicles available in the industry for use as a qualification vehicle, or you can design your own vehicle. Other vehicles include:

- Boeing qualification board (primarily PTH)
- NASA Test Assembly (mixed technology)
- Low Residue Soldering Task Force (LRSTF) test assembly (mixed technology)
- ARPA ETC'96 Test Board (mixed technology)
- Series of boards from TopLine (e.g. Sabre boards)
- Solectron board
- Not recommended - IPC-B-24, IPC-B-25, IPC-B-25A

Whatever is chosen, the vehicle must have the following characteristics.

- The vehicle must be representative of the product and be amenable to SIR testing
- The test patterns and components must be representative of the hardest / greatest challenge on your product, e.g. if you do 15 mil pitch SMT, your test vehicle should have 15 mil pitch.
- It should contain the same material mix as on your product, e.g. if your product has tin-lead SMOBC on FR-4, your test vehicle should too.
- The SIR test patterns under the components must not be covered with solder mask

You will need to know the number of “squares” in the representative SIR test patterns to determine the SIR pass fail numbers related back to the IPC-B-36 test board.

Solder Mask and Metalization

Now you have your fabricator chosen and your fabricator now has your Gerber files for the test board in hand. You must choose the solder mask and metalization that will go on your test assembly. At this point, the following question will probably be raised:

“Do I need to do qualification testing for every combination of solder mask and metalization?”

Again, potentially yes and potentially very expensive. Just as before, you should look very hard at your mix of solder masks. Do you really need that many? The same thought applies for the metalization involved. If most of your product is liquid photoimageable (LPI), then that is what should go on your vehicle. If most of your product is HASLed, then your test vehicles should be as well.

The selection of solder mask and metalization should be from a designed study. If you are trying to use the “worst case” approach, a designed study is the only way to do so. At some point in the future, it is likely that your customer will want to see data on how you chose the mask-metalization combination for testing. A scientific study looks much better than showing them the dart board.

Fabricating the Vehicles

Now that you have chosen the fabricator, laminate, solder mask, and metalization, it is time for your fabricator to make the test boards. The boards should be made in the same way as your product. There must also be no special cleaning steps (precleaning) that are not part of the normal fabrication process.

You will need to know the number of boards to be made. You will need to have 10 test samples for each combination of materials and processes that you wish to qualify. Example: if you have chosen one product line of CEM-1, LPI mask, tin-lead and a second product line of FR-4, LPI mask, OSP coated, to go through your assembly process, then you will need 20 boards (at least). Ten boards for the first product line and ten boards for the second product line.

Since you get better prices from volume discounts, order lots. You can use the other boards for preliminary studies and for the inevitable goofs in manufacturing.

Assembly Process

Now you have the fabricated test boards, and presumably the test components, in house, ready to subject them to the assembly process. The rule to follow is “if your product sees it, the test board sees it”. This includes exposure to mounting adhesives, temporary solder masks, solder paste, solder flux, hand soldering with cored wire solder (and additional flux if that’s what you do on product). Any interim cleaning steps, such as brushing with isopropanol, or a final cleaning prior to conformal coating, must also be performed.

Conformal Coating

Now the manufacturer must choose whether or not to conformally coat the test boards. If the product is coated, the test board is coated. If you do not conformally coat the product, then the test board is not coated. Again, you face the potential of having to do the testing for all your coatings, and determining if you need all those coatings. Each coating can represent a harmful interaction with existing residues. Only preliminary studies can determine if there are hazardous situations with any of your coatings or coating processes.

One note of caution from a test lab professional, if you coat the entire board, including the points we need to attach to for SIR testing, and we have to then scrape the coating off to get a good connection, we scream loudly and go for your pocketbook. You may need to mask off these connection points during the coating process or include test lead attachment as part of the assembly process. A competent test lab should be able to assist with this area (I know of a good one in Kokomo).

The Test Environment

The last choice the manufacturer has is the choice of the SIR test environment: cyclic or static. The cyclic method has the environment cycle between 25C and 65C, 90% RH, three times per

day, for ten days. This method simulates a condensing environment and is most applicable to conformally coated product, or uncoated product that will likely see condensation during its life cycle. The static method has a constant 65C / 85% RH environment over a 7 day period. This method is more applicable for testing for corrosion and metal migration in uncoated product, or for product where condensation is not likely.

While the choice is up to the manufacturer, it is recommended that the coated boards be tested with the cyclic profile and the uncoated boards be tested with the static method.

The SIR Test

Unfortunately, SIR testing is still a technique dependent test. IPC-9201 can help educate both the tester and the manufacturer on the many factors which affect SIR testing. This becomes important now because the pass-fail criteria for SIR testing includes the variability of your data set as a factor. In previous SIR qualification protocols, all you were concerned about was a minimum value. If you had a wide variation to the data, it did not make a difference. Now it does. The pass-fail criteria looks at both minimum values and the standard deviation of the data set.

Choose a test lab that knows SIR testing well. They should be able to show you how controlled their chambers are; repeatability studies for SIR, calibration data for SIR, chamber water cleanliness, etc.

Why should you be concerned about all of these things? If your SIR tester does not know what he/she is doing, the test variability can overshadow all the work you have done in the process development. A poor test technique could fail your qualification more than your process parameters.

Calculating the Pass Fail Criteria

All of the pass-fail SIR criteria for J1B is related back to a comparable pattern on the IPC-B-36 test board. Let us say that we use a simple test PWB with only one SIR pattern per PWA; a "Y" pattern under the most difficult to clean part on each test assembly. This "Y" pattern has a "gap"

$$25.4 \text{ mm long} * .635 \text{ mm spacing} = 25.4/0.635 = 40 \text{ squares}$$
$$(1 \text{ inch long} * 0.025 \text{ inch spacing} = 40 \text{ squares})$$

The equivalent pattern for a B-36 would be pattern M6, M7, M9, or M10. Each of these patterns have the same pattern characteristics:

$$68.58 \text{ mm long} * 0.152 \text{ mm spacing} = 68.58 / 0.152 = 450 \text{ squares}$$
$$(2.7" \text{ long} * 0.006" \text{ spacing})$$

Our new pass-fail level for our "Y" pattern = 100 megohms * (450 / 40) = 1,125 megohms or 9.05 on the log scale.

Example Data Set

Process	PWA	T0	M1	M2	M3	M4	M5	M6	M7	TF
C	101	3.21E+13	6.54E+10	5.16E+10	4.65E+10	4.10E+10	3.39E+10	2.75E+10	2.26E+10	7.77E+11
C	102	7.08E+12	2.01E+10	2.23E+10	2.17E+10	2.01E+10	1.86E+10	1.69E+10	1.56E+10	1.12E+12
C	103	1.21E+12	4.00E+09	4.23E+09	4.18E+09	4.23E+09	4.14E+09	4.09E+09	4.03E+09	4.68E+11
C	104	4.21E+11	1.32E+10	1.56E+10	1.51E+10	1.45E+10	1.38E+10	1.32E+10	1.29E+10	1.78E+12
C	105	9.40E+11	1.16E+10	1.18E+10	1.05E+10	9.57E+09	8.74E+09	7.98E+09	7.45E+09	5.09E+11
C	106	3.62E+13	2.94E+10	1.33E+10	6.30E+09	4.56E+09	3.04E+09	2.85E+09	2.86E+09	1.13E+12
C	107	6.73E+12	6.24E+11	3.57E+11	4.31E+10	1.63E+10	9.59E+09	7.90E+09	6.91E+09	3.42E+12
C	108	7.33E+12	6.12E+11	1.94E+11	8.96E+10	5.65E+10	4.13E+10	2.80E+10	2.28E+10	3.08E+12
C	109	5.13E+12	1.83E+10	1.65E+10	1.53E+10	1.45E+10	1.37E+10	1.29E+10	1.27E+10	3.49E+12
C	110	8.26E+11	1.03E+10	1.25E+10	1.17E+10	1.10E+10	1.01E+10	9.42E+09	9.05E+09	4.66E+13

Let us say that the above table is the data generated for our 10 test boards. T_0 represents initial ambient measurements. T_f represents final ambient measurements. All other measurements are made at the elevated temperature and humidity conditions of the chosen test method. We are interested only in the minimum values for the test pattern over the course of the test. Those values appear in bold face. If we made a table of these minimum (also called WetMin) numbers, we would have the following.

Process	PWA	WetMin	LogOhm
C	101	2.26E+10	10.35
C	102	1.56E+10	10.20
C	103	4.00E+09	9.60
C	104	1.29E+10	10.11
C	105	7.45E+09	9.87
C	106	2.85E+09	9.45
C	107	6.91E+09	9.83
C	108	2.28E+10	10.36
C	109	1.27E+10	10.10
C	110	9.05E+09	9.96
		Mean	9.98
		Standard Deviation	0.30

From the geometric mean of the WetMin values (9.98) we subtract three standard deviations:

$$9.98 - 3*(0.30) = 9.08.$$

Our calculated pass-fail number is 9.05. Since $9.08 > 9.05$, our candidate process passes the test, at least numerically. If there is corrosion or metal migration (which bridges more than 20% of the spacing) found on the SIR test pattern after testing, then the test fails.

Summary of Choices to Be Made

The choices facing the assembler qualifying to J-STD-001B are:

- selection of fabricator
- selection of test vehicle and SIR patterns on test vehicle

- selection of metalization
- selection of solder mask
- selection of assembly process parameters
- selection of coated or uncoated samples
- selection of the SIR temperature - humidity profile

Each selection can have a major impact on both the qualification testing and on your product. Each selection should reflect the choices made for actual hardware.

Summary of Preliminary Studies Recommended

For the assembler facing this array of choices, I recommend the following preliminary studies:

- Bare board cleanliness study for the fabricators by ion chromatography. The use of the classical ionic cleanliness testers will not give you enough relevant information.
- Compatibility studies between masks / metalizations and your assembly process. Both SIR and ion chromatography can be used for this.
- Investigate different SIR vehicles to determine which is most representative of your product and to establish baseline responses for the vehicle.
- Do some dry runs on a limited number of samples to see if you are near passive, before doing a large scale qualification test.
- If you are a large corporation, or use a high mix of materials, ask yourself candidly if you really need that many materials.

Other Resources Available

The new approach to process qualification will undoubtedly bewilder many people (it bewildered me, and I helped write it). Here are some other resources to aid in your background investigations:

- Drafts of the IPC-J-STD-001 Handbook (will eventually compliment the standard when completed)
- Course - Understanding the Importance of the National Soldering Standard - taught by Rosser, Hymes, and Maguire
- IPC-TR-1090, "The Layman's Guide to Qualifying New Fluxes to MIL-STD-2000A and J-STD-001A"
- IPC-TR-467
- EMPF No-Clean Technology Course
- A second "Layman's Guide" for J1B. I anticipate finishing it in March of 97.