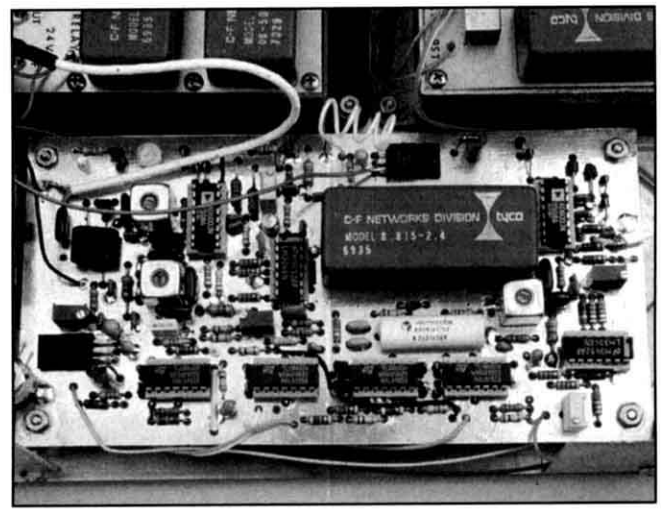
By Bill Carver, K6OLG

A High-Performance AGC/IF Subsystem

If you're looking for exceptional receiver performance, you need an exceptional IF and AGC system—like this one.



A great deal of emphasis has been placed on the ability of a receiver's front end to cope with multiple strong signals. Less has been published on the IF/AGC system of the receiver, despite the fact it determines how *every* signal sounds. This article covers that important territory.

The IF/AGC subsystem shown in Figure 1 has a minimum discernible signal (MDS) level of 0.03 µV in a 2.5-kHz bandwidth, and its AGC can be set to have a few decibels rise in audio with a range of signal amplitudes of less than 0.1 µV to over 0.2 V. The input-intercept point is about +20 dBm, so in-band intermodulation distortion (IMD) is 40 dB down even for S9 + 70-dB signals. The constant-gain time interval of the "hang" AGC circuit is smoothly and continuously varied from 100 ms to 2 seconds using a panel-mounted knob. This IF/AGC system is intended for use with a front end having a net gain of +3 dB and a 6-dB noise figure (NF), and directly drives a +7-dBm diode-mixer product detector.

My receiver's IF is 4.434 MHz, using ladder filters made of European color-burst crystals. This circuit also works at 9 MHz, a popular IF, with a few different capacitor values and a different number of turns on L1, L2 and T2. Coil design for these two frequencies is given, but you can adapt it to any high frequency.

AGC Basics

An amplifier with feedback to control its gain can be resolved into two components: the amplifier itself and the detector and processing circuits that develop the gain-control feedback voltage.

The Analog Devices AD600 is a dual, low-noise, wideband, variable-gain amplifier IC. The gains of the two internal 40-dB amplifiers are controlled by the potential difference between the C*x*LO (that is, C1LO or C2LO) and C*x*HI (C1HI or C2HI) pins. This IC has about a 40-dB gain-control range with a *constant* gain-control scale factor of 32 dB/V. C*x*LO voltage above or below the 0.625-V difference leaves the gain at 0 or 40 dB, respectively. With a 2-dB NF and 30-MHz bandwidth, it's ideal for the gain portion of an IF system.

The logarithmic envelope detectors produce a 3-V output change from an 8-dB input signal change, a scale factor of 0.375 V/dB. Coupled with the AD600, this produces a loop gain of 12, which means an input-signal change causes an output-signal change equal to the input-signal change divided by 13. For example, a 65-dB input-signal change results in a 5-dB output-signal change.

Two AGC Detectors?

Wideband noise at the AGC detector would preclude using AGC for low signal levels; the amplifier's noise bandwidth must be limited. But the time delay of a filter placed between controlled stages and the AGC detector destabilizes an AGC system, so AGC voltage to the gain-controlled stages ahead of the filter must be delayed. This permits brief clipping of large signals and envelope distortion at the leading edge of a signal.

This amplifier system uses *two* AGC detectors. The first one, called FAST, reduces the gain of the stages ahead of the noise filter, preventing them from clipping until the SLOW detector—placed after the filter—can catch up. This prevents overloading U1A-U1B for signal levels above 10 µV for a few milliseconds until the SLOW AGC responds. This "minor" detail makes a big difference in how a receiver sounds even though most ears can't identify *why*.

Identical FAST and SLOW detectors operating at the same signal level—combined with the well-defined gain control characteristics of each AD600—permit seamless combination of the detector outputs. Q2's gain is adjusted so both detectors have the same signal voltage when U2A's gain is at minimum.

The JFET and First Three AD600 Amplifier Stages

The AGC threshold occurs when a signal level of –32 dBm appears at the output of U2B. This results from an input-signal level of about –128 dBm (0.09 µV) when the signal-to-noise ratio (S/N) is approaching 10 dB. Maximum signal is reached with –20 dBm at the output of U2B, corresponding to an input-signal level of 0 dBm (0.23 V).

Q1 is a J310 FET with gate-source transformer feedback. Its theory of operation is covered by Wes Hayward, W7ZOI, in *Introduction to RF Design*;[1] an almost identical implementation to this one was described by Colin Horrabin, G3SBI, in the *Technical Topics* column of the May 1995 issue of *Radio Communications*.[2]

Q1's gain is 12 dB and is set by the 2:1 transformer (T2), the load resistance of the following stage and the 221-Ω metal-film

[1]Notes appear on page 44.

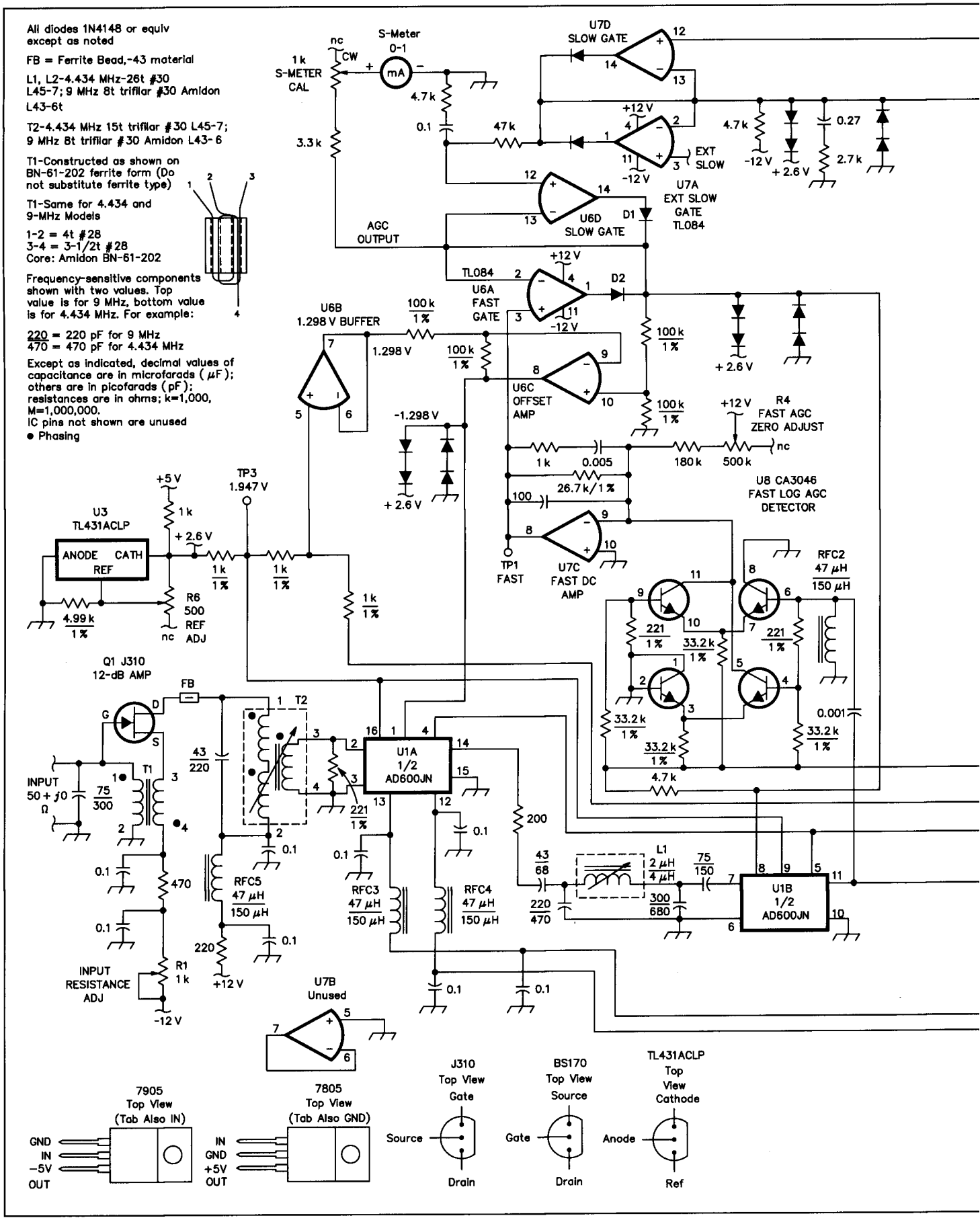
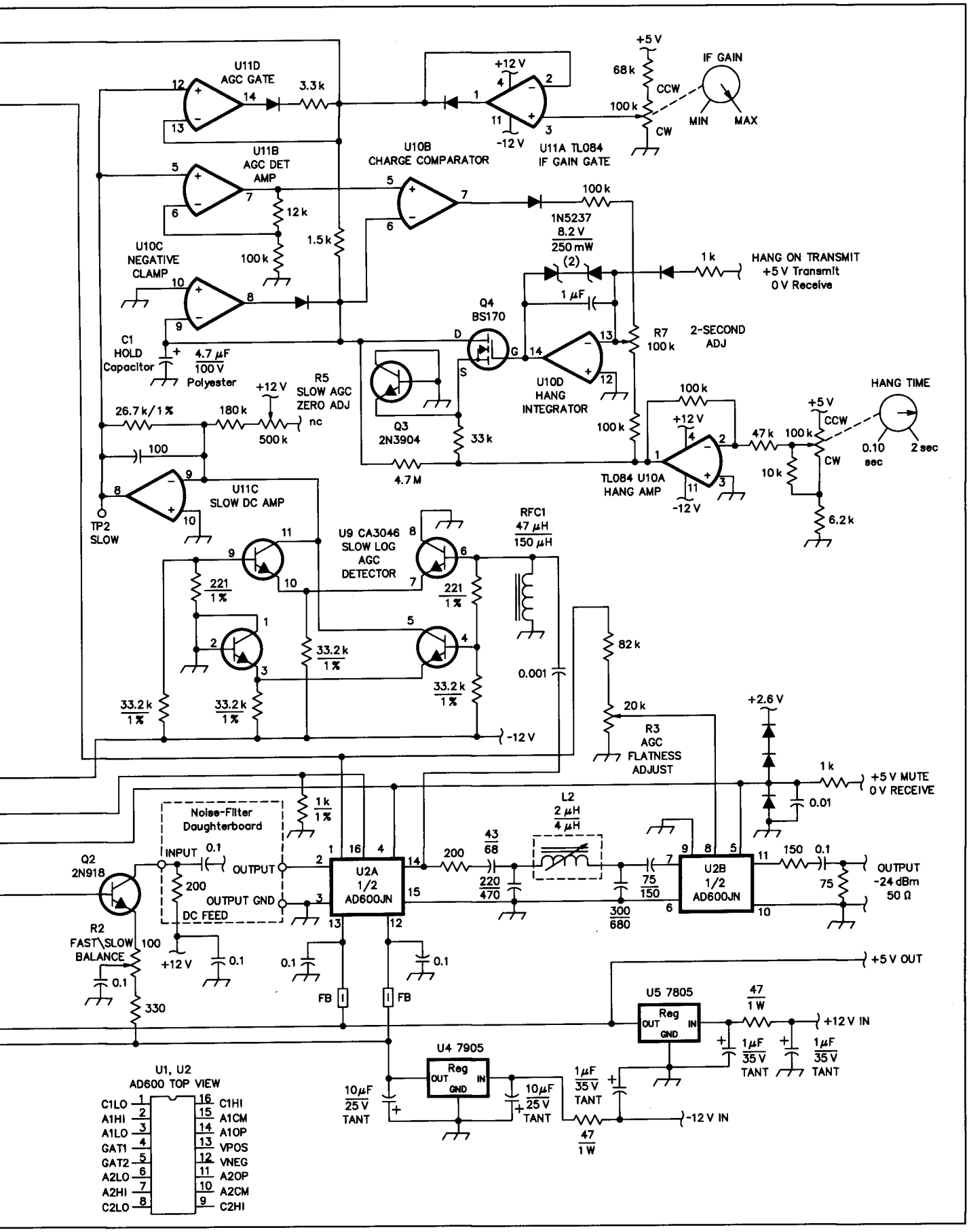


Figure 1—Schematic of the IF/AGC circuit. Where two values for a component are shown—one above and one below a short horizontal line—the upper value is for use at an IF of 9 MHz, the lower one for a 4.434-MHz IF. U8 and U9 are shown uncharacteristically here so as to provide a better understanding of circuit operation. FB-43-101 ferrite beads can be used.


U11D
AGC GATE
3.3 k
+12 V
-12 V
U11A TL084
IF GAIN GATE
+5 V
68 k
IF GAIN
CCW
100 k
CW
MIN
MAX
U11B
AGC DET
AMP
12 k
1.5 k
100 k
U10B
CHARGE COMPARATOR
100 k
1N5237
8.2 V
250 mW
(2)
1 k
HANG ON TRANSMIT
+5 V Transmit
0 V Receive
U10C
NEGATIVE
CLAMP
Q4
BS170
1 µF
R7
100 k
2-SECOND
ADJ
C1
HOLD
Capacitor
4.7 µF
100 V
Polyester
R5
SLOW AGC
ZERO ADJ
nc
500 k
26.7 k/1 %
180 k
+12 V
100
Q3
2N3904
33 k
4.7 M
U10D
HANG
INTEGRATOR
100 k
+12 V
47 k
100 k
+5 V
CCW
CW
10 k
6.2 k
HANG TIME
0.10
sec
2 sec
TL084 U10A
HANG AMP
-12 V
U11C
SLOW DC AMP
TP2
SLOW
U9 CA3046
SLOW LOG
AGC
DETECTOR
RFC1
47 µH
150 µH
221
1 %
33.2 k
1 %
0.001
82 k
20 k
R3
AGC
FLATNESS
ADJUST
+2.6 V
1 k
+5 V MUTE
0 V RECEIVE
0.01
Noise-Filter
Daughterboard
INPUT
0.1
OUTPUT
200
OUTPUT GND
DC FEED
Q2
2N918
R2
FAST SLOW
BALANCE
100
330
+12 V
0.1
U2A
1/2
AD600JN
L2
2 µH
4 µH
43
68
220
470
300
680
75
150
U2B
1/2
AD600JN
150
0.1
75
OUTPUT
-24 dBm
50 Ω
FB
+5 V OUT
U5 7805
Reg
OUT
GND
IN
47
1 W
+12 V IN
1 µF
35 V
TANT
U4 7905
10 µF
25 V
TANT
-12 V IN
U1, U2
AD600 TOP VIEW
C1LO 1
A1HI 2
A1LO 3
GAT1 4
GAT2 5
A2LO 6
A2HI 7
C2LO 8
16 C1HI
15 A1CM
14 A1OP
13 VPOS
12 VNEG
11 A2OP
10 A2CM
9 C2HI

resistor. The resistor value is optimized for the lowest AD600 noise figure. To produce a precise 50-Ω input resistance, Q1's source current is adjustable and a capacitor across the input terminals cancels the leakage reactance of the feedback transformer, T1. Minimum transformer loss is necessary to achieve a low noise figure, so the input transformer (T1) *must* be wound exactly as shown on a BN-61-202 balun core.

There are four amplifier stages in two AD600 packages. The first 40 dB of gain reduction is done only by the third stage; the next 40 dB in the second stage, and only the last 40-dB reduction applied causes any gain reduction in the first stage. As AGC voltage passes halfway between the threshold of adjacent stages, gain control is being handed off from one IC to the next. This sequential gain reduction maximizes signal-to-noise ratio (S/N).

To fully understand the AD600, you'll need a data sheet.[3] But briefly, as the AD600's C*x*LO control voltage (either C1LO or C2LO) changes from –0.625 to +0.625 V with respect to its C*x*HI, its gain changes linearly from +40 dB to 0 dB (unity gain).

Because C1HI of U2A is biased to 0.649 V, its gain will change by 40 dB as the AGC voltage at U7 pins 2 and 13 changes from 0.024 to 1.274 V. C2HI of U1B is at 1.947 V, so its gain will change by 40 dB as the AGC voltage at U6 pins 2 and 13 changes from 1.322 to 2.572 V The small gap between 1.274 and 1.322 V provides a smooth transition of gain control from U2A to U1B, as explained in the AD600 data sheet.

The threshold of U1A is also 1.947 V, but 1.298 V is subtracted from the AGC voltage by U6C. Thus, the 40-dB gain change of U1A occurs as the AGC voltage changes from 2.620 to 3.870 V. Taken together, as the AGC voltage at TP2 varies from 0 to 3.870 V, the gain of the three cascaded stages changes by 120 dB, with gain reduction starting at the last amplifier stage.

Noise Filter

The homebrew crystal-ladder filter between the second and third AD600 stages is not intended for selectivity. This filter removes the broadband noise generated by Q1 and U1, permitting a lower AGC threshold. The filter is 2500 Hz wide at the –3 dB points, and 5500 Hz wide at the –20 dB points, removing much of the noise from the opposite side of zero beat, improving the IF NF and thus the overall receiver NF. Selectivity should be accomplished *ahead* of this IF strip.

After measuring the series resistance and motional inductance of your crystals, ladder-filter design becomes essentially a cookbook process using the *X* software bound with Wes Hayward's *Introduction to RF Design*. At 4.43 MHz, the usual crystal-ladder filter cannot be made 3 kHz wide. Hayward's *Refinements in Crystal Ladder Filter Design* in the June 1995 issue of *QEX*[4] shows how the holder capacitance of each crystal can be parallel-tuned to permit construction of SSB-width filters.

Figure 2 shows the ladder filter. The middle crystal is parallel tuned as Hayward suggests. However I "neutralized" the capacitance of the input and output crystals with a phase-inverting transformer, self-resonant at the IF. Winding information is given for 4.434 MHz. Small trimmer capacitors could have been used to precisely adjust the neutralization, but fixed-value 3.3-pF capacitors work well and eliminate some adjustments.

At the 2500-Hz bandwidth, the filter impedance is 2.9 kΩ. **L** networks are used at each end to match the filter to the 100-Ω input impedance of U2A at one end, and the 200-Ω collector resistor of Q2 at the other end. Every set of crystals will be different; exact values for the **L** networks must be determined after the filter impedance has been computed by Hayward's *X* program. Once the filter is designed, breadboard it and verify proper operation before committing parts to a PC board.

At 9 MHz, neither parallel tuning nor neutralizing is necessary to get the SSB bandwidth, and if used only for receiving digital modes, you can even omit the neutralization at 4.434 MHz. Making a three-pole filter sounds more difficult than it is: With the *X* program and one of the many tutorial articles on ladder filters, it's a tedious snap.

I anticipate that many will choose to use a commercial filter instead of homebrewing a ladder filter. There's enough gain in Q2 to absorb a filter loss of up to 10 dB. Q2's 200-Ω collector resistor value can be increased to about 330 Ω to match a commercial filter's impedance and eliminate one **L** network.

Using more filter poles and/or narrower filters may require increasing the value of C2 to delay the SLOW AGC more than the filter delay, although Harold Johnson, W4ZCB, didn't find this necessary with an eight-pole SSB-width filter he used.

Forward Gain Correction of the Output

The fourth AD600 stage, U2B, is outside the AGC loop. A signal 130 dB above threshold causes the OFFSET SLOW AGC voltage at TP4 to increase from its zero-signal value of –0.625 V to 3.125 V, and with a loop gain of 13, the output of U2A has *increased* by about 10 dB. When about 10% of the OFFSET SLOW AGC voltage is applied to U2B's C2LO pin, its gain *decreases* by 10 dB, resulting in no signal change at its output.

R3 can be adjusted so the output is flat within a few decibels for signal levels of 0.23 µV to 0.23 V (–120 dBm to 0 dBm). Because of finite S/N for small signals, it's not possible to compensate perfectly, but the resulting flatness is remarkable—and addictive. Some may prefer the audio level to rise somewhat with increasing signal. R3 allows adjustment of U2B's contribution to gain control to suit each builder's taste.

The output of U2B is attenuated by a 150/75-Ω resistor pair to produce a –26 dBm signal level and 50-Ω output resistance perfect for the +7-dBm diode-mixer product detector. U2B and the resistors produce low IMD and a high S/N from the product detector while preventing BFO signal leakage to the SLOW detector.

Reference-Voltage Details

U3 is a TL431 shunt regulator whose 2.6-V output is divided by four identical 1%-tolerance resistors to produce three close-tolerance voltages with only one adjustment: 1.947 V for the C1HI threshold for U1A and U2B; 1.298 V to offset the AGC voltage for U1A and 0.649 V for the threshold of U2B. R6 is adjusted to produce 1.947 V at TP3. The 1%-tolerance resistors need only have the same value—between 1 kΩ and 5 kΩ. DigiKey[5] and other suppliers offer suitable resistors at a modest price.

The AD600 C*x*LO and MUTE pins have 15 small-signal silicon diodes clamping the pins to ground or to the 2.6-V potential at U3. Normally, the diodes won't conduct. They're there to prevent damage to the expensive AD600s in case of misconnection, loss of a power supply or op-amp failure. Being a shunt regulator rather than a three-terminal regulator, U3 is able to sink diode current should a fault occur.

The AGC Detectors

The two AGC detectors, U8/U7C and U9/U11C are not rectifiers, but an interconnection of matched transistors that produce an average current equal to the logarithm of the applied IF signal over a range of signals. These detectors produce several dc volts from only 10 mV of signal, and their logarithmic characteristic complements the AD600 scale factor almost perfectly.

Processing the AGC Voltages

The large number of op amps makes this circuit look complex. But the ideal performance of op amps isolates each component's contribution to the circuit making it easier to understand and troubleshoot than it may appear.

The SLOW detector output at TP2 and the **IF GAIN** potentiometer voltage at U11A pin 3 are gated by U11A and U11D. Whichever one has the higher voltage charges the **HOLD** capacitor, C1, through its diode and a 4.7-kΩ resistor. The output pin of the amplifier whose input is lower (not in control of the output) will swing to about –11 V. This bizarre action is perfectly normal and logical, but takes some getting used to when troubleshooting. Similar action occurs at U6A-U6D and U7A-U7D.

The output from U11A-U11D is combined with an external AGC signal (if present) in U7A-U7D. Whichever signal is higher appears at U7 pins 2 and 13, and controls the gain of U2A. The output of U7A-U7D is combined with the FAST AGC detector output in U6A and U6D to control the gain of U1B and drive the S meter. Buffered by U6B, 1.298 V is subtracted from the combined detector outputs in U6C to become the

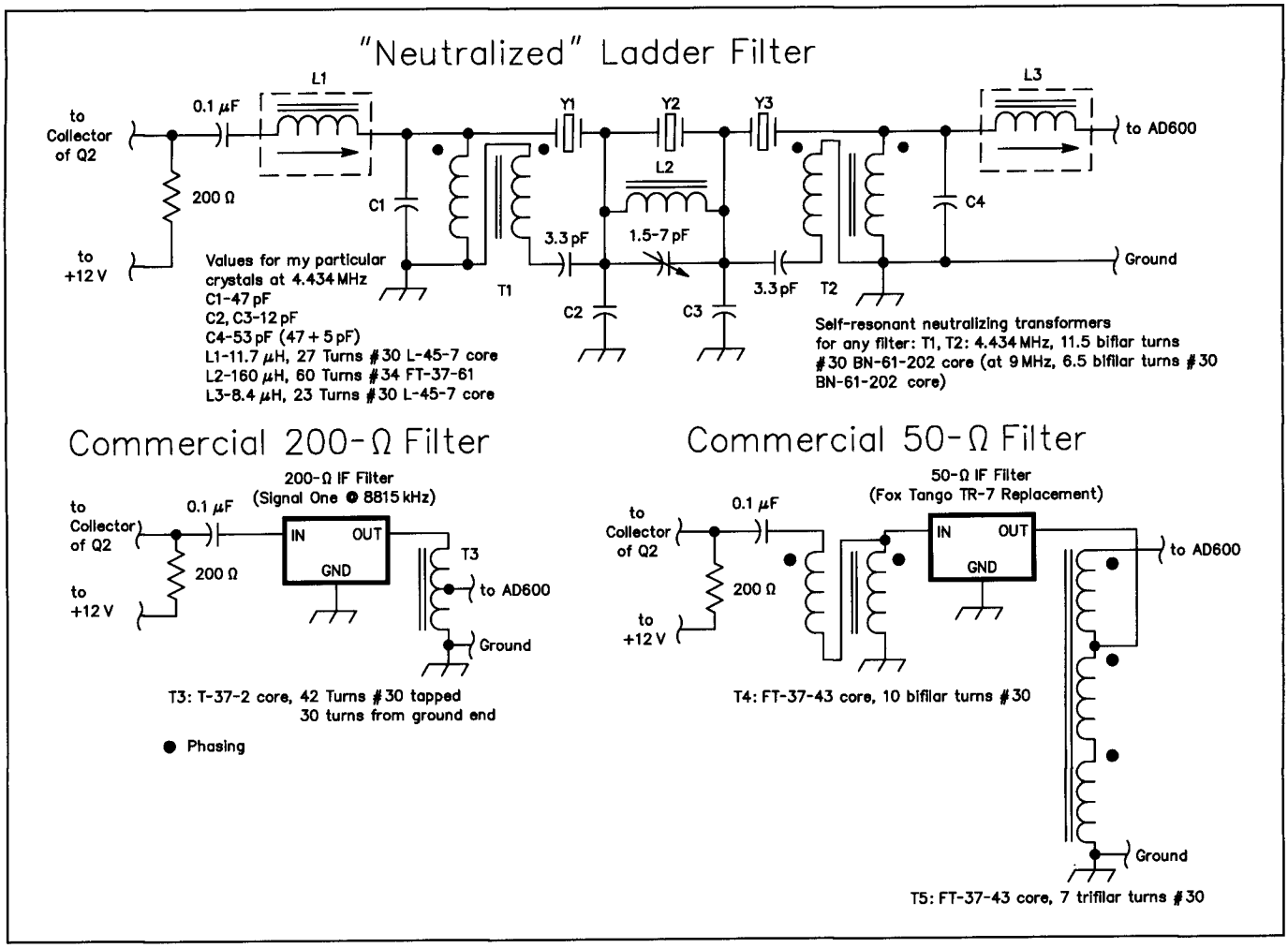


Figure 2—Example filter designs.

OFFSET AGC voltage with a total swing of –1.2 to 2.6 V appearing at U1A pin 1 to control its gain.

Hanging AGC

When the SLOW detector output is more than 90% of the voltage on C1, U10B's output (pin 7) will be about 11 V. Current through the 47-kΩ resistor and diode to U10D pin 13 charges the 1-µF integration capacitor, C1, its output moving toward the negative supply until the 1N5237 Zener diode starts to conduct with about –8 V at pin 14 of U10D. Q4 is cut off by the negative base voltage and no drain current flows to discharge C1. The 4.7-MΩ resistor slowly discharges C1, permitting the AGC to track modest amounts of fading with Q4 cut off. Clamp U10C provides current as necessary to keep Q4 from developing a negative voltage on C1.

When the slow AGC detector voltage is *not* 90% of the voltage on C1, U10B's output is negative and the integrator output swings in the positive direction at a rate determined by the setting of the **HANG TIME** potentiometer. It stops charging when C1 is discharged by Q4 down to 90% of signals-plus-background noise, or the other 1N5237 starts to conduct with 8 V on pin 14 of U10D. When the **HANG TIME** pot is fully clockwise, it not only takes a longer time for receiver gain to return, it returns at a slower rate.

S Meter

The linear-in-decibel nature of the AD600 AGC voltage means the 0 to 3.87-V swing at TP2 corresponds to a 120-dB gain change, plus the signal rise at the output of U2A, a total of about 130 dB. The AGC voltage is almost perfectly logarithmic or linear in S-units over this range.

Multiplier resistors develop a 1-mA meter current for 3.75 V at TP2. With appropriate changes to the resistors, more sensitive meter movements can be used. It's convenient to have a portion of the multiplier adjustable; I set my meter so the needle is vertical for an S9 signal.

It's incredible that the S meters of $4000+ transceivers sold today indicate the signal strength has changed when a preamp or attenuator is switched in! The linearity of the AD600 permits the S-meter reading *to be corrected* for the gain of a preamp or loss in a switched attenuator. For example, the voltage across the coil of a relay used to switch an attenuator can be fed to the S-meter through a variable resistor. So, the reduction in AGC voltage caused by the attenuator is perfectly compensated for by current developed from the coil voltage.

I incorporated this idea in the breadboard version, but the number of possible attenuator and preamp combinations suggested quickly became clumsy. Then, I realized that current from a digital-to-analog converter (DAC) could compensate for *all* possible preamp/attenuator combinations—and even adjust the S-meter reading on a per-band basis to compensate for slightly different gains on each band. This most-general approach requires *no* additional components and was quickly adopted.

Adjustment

Seven potentiometers need adjustment. The adjustments don't interact, and six of them are quick and easy to make.

• Using a noise bridge (or other suitable impedance-measuring instrument), set the input resistance to 50 Ω with R1.

R1 had sufficient range to handle all the J308s and J310s from several batches in the handful of amplifiers built by W4ZCB and me. A ground connection is provided at the top side of T1 so an additional *half* turn can be added to the 1-2 winding of T1 if varying R1 won't produce the proper input-resistance value. The input reactance should be

very close to zero. At frequencies other than 4.434 or 9 MHz, scale the input-capacitor's value and verify zero reactance using a noise bridge.

• Set R6 for 1.947 V at TP3. The potential at U6B pin 7 should be very close to 1.298 V, (1.272 min, 1.324 max). The voltage at U2 pin 16 should be close to 0.649 V (0.636 min, 0.662 max).

• Turn the **IF GAIN** pot fully counterclockwise, to minimum gain. Adjust R5 for 0 V at TP2, then adjust R4 to 0V at TP1.

• Turn the **IF GAIN** control clockwise, and connect a signal generator to the input. Peak T2, L1 and L2 for maximum gain. These are broad-tuning, low-Q circuits. Adjust the noise filter **L**-networks and verify the expected filter bandwidth.

• Apply sufficient signal to produce more than 1.6 V at TP1. Adjust R2 so that the voltage at TP1 decreases slightly. This is the only tricky adjustment; don't be surprised if you have to repeat it several times before you get it right. Midscale S-meter linearity depends on proper balance of the two detectors. Large changes in the S-meter reading for small signal changes of around 10 μV is a sure sign that R2 is *not* adjusted properly.

• Connect a pulsed test signal to the input. (Receiving the signal from a keyed transmitter connected to a dummy load will do.) Turn the **HANG TIME** potentiometer clockwise to its two-second position. Adjust R7 for a two-second delay between the end of the signal and the beginning of the voltage drop at AGC OUTPUT.

• Adjust R3 (**FLATNESS**) to suit your taste. This can be done by ear—while listening to an on-the-air roundtable for example—or by using a signal generator and test instruments.

Little Details

This amplifier is insensitive to exact supply voltage, but the supply voltage needs to be *stable* so that the zero adjustments R4 and R5 will be stable. The +12 and –12 V potentials are supplied by off-board 7812 and 7912 regulators, respectively.

The 10-kΩ resistor between the **HANG TIME** pot's wiper and the pot's low end simulates an audio-taper pot (these are hard to find!), providing the proper feel with a common linear-taper control. The **IF GAIN** control is also a linear-taper control. For computer control, both **HANG** and **IF GAIN** can be controlled by a 0 to 5-V dc signal from a digital-to-analog converter.

The 150-μH RF chokes are parallel resonant near the IF. RF choke values of 100 to 200 μH will have virtually identical performance at 4.434 MHz. At 9 MHz, values between 27 and 47 μH are suitable. There need be no fear of substitution.

The 9-MHz unit was built using Amidon L-43-6 slug-tuned coil forms. The 4.434-MHz version uses L-45-7 forms from Lodestone Pacific.[6] These forms have a Q about 20% higher than the L-43 forms and are physically sturdier. Because coil Q is of little concern in this project, Amidon L-43-6 forms can be used at 4.434 MHz with minor adjustments to the number of turns.

Because of fading, on-the-air signals are not an ideal source of test signals. A keyed transmitter, *known to have a good keying envelope*, can be used with an oscilloscope to confirm proper circuit operation. Or, you can use a diode mixer with a signal generator tied to the RF port, drive the dc-coupled IF port with a pulse generator and take the output from the LO port. In his October 1995 *QEX* article,[7] Mark Mandelkern, KN5S, showed circuits used with an HP-8640 to produce test signals.

Transmit Hang, Diversity Reception and External AGC

A 5-V logic potential during transmit forces the hang integrator output to –10 V and C1 discharges slowly through the 4.7-MΩ resistor during transmit intervals. In fast-break situations (full QSK CW, AMTOR and sometimes even SSB) this causes the receiver gain to return to nearly its previous level rather than full gain. C1 discharges to 0 V during longer transmissions.

With two IF strips and two mixers, connecting both SLOW to the EXT SLOW of the other gives gain control to the stronger signal, providing diversity reception to combat multipath reception on the digital modes. Some older, but very good Fredrick modems provide an AGC output that may benefit from the EXT SLOW connection.

Construction

I successfully used IC sockets at 4.434 and 9 MHz on an "ugly" groundplane breadboard, and with several iterations of PC-board layout. On the other hand, an etched and drilled PC board saves a lot of time.[8] Like the hand-wired board described earlier, the PC board is double-sided with a ground plane and the components on top, traces on the bottom. To minimize cost, the board doesn't have plated-through holes; component leads and grounded socket pins are soldered directly to the ground plane.

Although this amplifier is stable even as a breadboard, remember that it has a lot of gain. Its stability can become marginal with scope probes radiating signals at amplifier outputs. Given the opportunity, the amplifier can pick up the BFO signal. I eliminated this possibility by placing the BFO and product detector in a shielded box. In the final package, each circuit should be in its own shielded box and *no* BFO signal should be detectable in the IF output.

Acknowledgments

Harold Johnson, W4ZCB, is a very active partner. After our design discussions, he checked circuits, built the 9-MHz version and proved himself to be a dynamite proofreader. Colin Horrabin, G3SBI, now working on a low-phase-noise synthesizer, contributed his thoughts via Internet, transatlantic telephone calls and mail. Wes Hayward, W7ZOI, has been a source of insight for this and other projects. During a telephone conversation many years ago, Wes first suggested using the AD600.

Notes

[1]Wes Hayward, W7ZOI, *Introduction to RF Design* (Newington: ARRL, 1994); see the *ARRL Publications Catalog* elsewhere in this issue.

[2]Colin Horrabin, G3SBI, Technical Topics, *Radio Communications*, May 1995, p 61.

[3]Analog Devices, One Technology Way, Norwood, MA 02062-9106; tel 617-329-4700; fax 617-326-8703. Data sheets can be obtained by a fax-back service, AnalogFAX: 800-446-6212; the AD600 data sheet faxcode is 1193. [Analog Devices data sheets are available as portable document files (.PDF file extension) on the Web at **http://www.analog.com.** You'll need *Adobe Acrobat* (free software available via a link) to view the files.—*Ed.*]

[4]Wes Hayward, W7ZOI, "Refinements in Crystal Ladder Filter Design," *QEX*, Jun 1995, pp 16 to 21.

[5]Digi-Key Corp, 701 Brooks Ave S, Thief River Falls, MN 56701-0677, tel 800-344-4539, 218-681-6674; fax 218-681-3380; on the Web at **http://www.digikey.com/**

[6]Lodestone Pacific, 4769 Wesley Dr, Anaheim, CA 92807; tel 714-970-0900; fax 714-970-0800. Minimum order is $25. Charge cards are not accepted. (Get the tuning tool for the coil slug while you're at it!)

[7]Mark Mandelkern, KN5S, "A High-Performance AGC System for Home-Brew Transceivers," *QEX*, Oct 1995, pp 12 to 22.

[8]A PC board for this project is available from FAR Circuits, 18N640 Field Ct, Dundee, IL 60118-9269, tel 847-836-9148 (voice and fax). Price: $18, plus $1.50 shipping for up to four boards. Visa and MasterCard accepted with a $3 service charge. (Note: FAR PC-board purchasers should request the following template, too.) A template package containing some assembly instructions, the PC-board pattern and a part overlay is available from the Technical Department Secretary, ARRL, 225 Main St, Newington, CT 06111. The price is $2 postpaid for ARRL members ($4 for nonmembers). Please identify your request for the CARVER IF/AGC CIRCUIT TEMPLATE.

Contact Bill Carver, K6OLG/7, at 690 Mahard Dr, Twin Falls, ID 83301, e-mail ***bcarver@magiclink.com****. Bill is an assistant professor at the College of Southern Idaho, where he teaches mathematics and engineering. In 1956, Bill picked up an* ARRL Handbook *and took it with him to Taiwan where he lived for awhile as a military dependent. After learning Morse Code, he got his Novice license (KN6OLG) in 1958 when he returned to the US. In 1964, Bill got his Extra Class ticket. Bill says it was the* ARRL Handbook *that encouraged him to build equipment and drove him to get an engineering degree (he received his BSEE in 1965 from the University of Nevada and his MSEE in 1970 from San Jose State). Primarily a digital operator, Bill enjoys 40-meter mobile CW, RTTY, AMTOR and Clover. Now Bill's got his first tower and hopes to augment homebrewing with a little more operating.*