High-Definition Multimedia Interface Specification

Informational Version 1.0

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Preface

Notice

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Document Revision History

1.0	2003/09/04	Initial Release of Informational Version

Intellectual Property Statement

Hitachi, Ltd., Matsushita Electric Industrial Co., Ltd., Philips Consumer Electronics International, B.V., Silicon Image, Inc., Sony Corporation, Thomson Inc., and Toshiba Corporation each may have patents and/or patent applications related to the High-Definition Multimedia Interface Specification. These companies intend to make available to the industry an Adopter Agreement that will include a limited, reciprocal patent license to certain of the electrical interfaces, mechanical interfaces, signals, signaling and coding protocols, and bus protocols described in the mandatory portions of the High-Definition Multimedia Interface Specification Release 1.0 published by HDMI Licensing, LLC.

Contact Information

The URL for the HDMI Founders web site is: http://www.HDMI.org.

Contribution

Silicon Image, Inc has made a significant contribution to this standard by editing the specification and developing the core technologies upon which this specification is based; including Transition Minimized Differential Signaling (TMDS®) technology.

Acknowledgement

HDMI founders acknowledge the concerted efforts of employees of Japan Aviation Electronics Industry, Limited and Molex Japan, who have made a significant contribution to this standard by developing the connector technology and the mechanical and electrical specifications for the required plugs and receptacles.

Table of Contents

Figures

Tables

1 Introduction

1.1 Purpose and Scope

This document constitutes the specification for the High-Definition Multimedia Interface (HDMI).

The High-Definition Multimedia Interface is provided for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays.

HDMI can carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats. Content protection technology is available.

HDMI can also carry control and status information in both directions.

This specification completely describes the interface such that one could implement a complete transmission and interconnect solution or any portion of the interface. The underlying Transition Minimized Differential Signaling (TMDS)-based protocol and associated electrical signaling is described in detail. The mechanical specification of the connector and the signal placement within the connector are described.

A device that is compliant with this specification is interoperable with other compliant devices through the configuration and implementation provided for in this specification.

Mechanical, electrical, behavioral and protocol requirements necessary for compliance are described for sources, sinks and cables.

1.2 Normative References

The following standards contain provisions that, through reference in this text, constitute normative provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. If the referenced standard is dated, the reader is advised to use the version specified.

EIA, EIA/CEA-861B, “A DTV Profile For Uncompressed High Speed Digital Interfaces”[1]

VESA, VESA E-EDID Standard, ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1, February 9, 2000

VESA, VESA E-DDC Standard, ENHANCED DISPLAY DATA CHANNEL STANDARD Version 1, September 2, 1999

Philips Semiconductors, The I^2C-bus Specification, Version 2.1, January 2000

ITU, ITU-R BT.601-5 Studio encoding parameters of digital television for standard 4:3 and wide-screen 16:9 aspect ratios (October 1995)

[1] All HDMI devices are required to comply with the requirements specified in EIA/CEA-861B except where specifically noted in this document.

ITU, ITU-R BT.709-4 Parameter values for the HDTV standards for production and international programme exchange (March 2000)

IEC, IEC 60958-1, “Digital audio interface – Part 1: General”, First edition 1999-12

IEC, IEC 60958-3, “Digital audio interface – Part 3: Consumer applications”, First edition 1999-12

IEC, IEC 61937, “Digital Audio - Interface for non-linear PCM encoded audio bitstreams applying IEC 60958”, First edition 2000-04

DDWG, “Digital Visual Interface,” Revision 1.0, April 2, 1999 (DVI)

1.3 Informative References

The following documents contain information that is useful in understanding this standard. Some of these documents are drafts of standards that may become normative references in a future release of this standard.

Digital Content Protection LLC, “High-bandwidth Digital Content Protection System Specification”, Revision 1.10 (HDCP)

ANSI/SMPTE, SMPTE Standard 170M (1999) for Television – Composite Analog Video Signal – NTSC for Studio Applications

ANSI/SMPTE, SMPTE Standard 274M

ANSI/SMPTE, SMPTE Standard 296M

EIA, CEB14, “Recommend Practice for use of EDID with EIA/CEA-861”

1.4 Organization of this document

This specification is organized as follows:

- Chapter 1 introduces HDMI, describes the purpose and scope of this document, references, organization of the document and usages and conventions.
- Chapter 2 defines terms and acronyms used throughout this document.
- Chapter 3 provides a high-level overview of the operation of HDMI.
- Chapter 4 describes the details of the Physical Layer of HDMI including basic electrical specifications and mechanical specifications of cables and connectors.
- Chapter 5 describes the Signaling and Encoding used by HDMI including descriptions of the different periods and encoding types used to transmit audio, video, and control data types and packet definitions for audio and auxiliary data.
- Chapter 6 describes Video related issues including video format timings, pixel encodings (RGB, YC_BC_R), colorimetry and corresponding requirements.
- Chapter 7 describes Audio related issues including audio clock regeneration, placement of audio samples within packets, packet timing requirements, audio sample rates and requirements, and channel/speaker assignments.
- Chapter 8 describes Control and Configuration functions, mechanisms and requirements, including use of the E-EDID, and InfoFrames.

- Appendix A describes the usage of Repeaters and Switches.
- Appendix B describes restrictions related to the use of the Type B connector.
- Appendix C describes DVI compatibility.
- Supplement 1 describes use of the Consumer Electronics Control (CEC) line and protocol.

1.5 Usages and Conventions

bit N	Bits are numbered in little-endian format, i.e. the least-significant bit of a byte or word is referred to as bit 0.
D[X:Y]	Bit field representation covering bit X to bit Y (inclusive) of value or field D.
0xNN	Hexadecimal representation of base-16 numbers are represented using 'C' language notation, preceded by '0x'.
0bNN	Binary (base-2) numbers are represented using 'C' language notation, preceded by '0b'.
NN	Decimal (base-10) numbers are represented using no additional prefixes or suffixes.

Within this specification, any descriptions of data structures, values or sequences that occur on the HDMI interface should be interpreted only as data structures, values and sequences that are transmitted by the HDMI Source. Due to the possibility of errors during the transmission, these items should not be construed as data structures, values or sequences that are guaranteed to be detected by the HDMI Sink.

2 Definitions

2.1 Conformance Levels

expected	A key word used to describe the behavior of the hardware or software in the design models *assumed* by this specification. Other hardware and software design models may also be implemented.
may	A key word that indicates flexibility of choice with *no implied preferenc*e.
shall	A key word indicating a mandatory requirement. Designers are *required* to implement all such mandatory requirements.
should	A key word indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase *is recommended*.
reserved fields	A set of bits within a data structure that are defined in this specification as reserved, and are not otherwise used. Implementations of this specification shall zero these fields. Future revisions of this specification, however, may define their usage.
reserved values	A set of values for a field that are defined in this specification as reserved, and are not otherwise used. Implementations of this specification shall not generate these values for the field. Future revisions of this specification, however, may define their usage.

2.2 Glossary of Terms

(Audio) Channel	Audio data meant to be delivered to a single audio speaker.
(Audio) Sample Clock	Original clock related to the audio input samples at the Source or the generated clock used to time the output of audio samples.
BCH	Error correction technique named after the developers: Bose, Chauduri, and Hocquenghem.
Byte	Eight bits of data.
Data Stream Disparity	Integer indicating “DC-offset” level of link. A positive value represents the excess number of “1”s that have been transmitted. A negative value represents the excess number of “0”s that have been transmitted.
Downstream	In the direction of the primary audio and video data flow, i.e. towards the Sink (e.g. display).
(HDMI) Source	A device with an HDMI output.
(HDMI) Sink	A device with an HDMI input.
(HDMI) Repeater	A device with one or more HDMI inputs and one or more HDMI outputs. Repeater devices shall simultaneously behave as both an HDMI Sink and an HDMI Source.

Multi-channel	Audio with more than 2 channels. Typically this term is applied to 6 (5.1) channel streams. Also called surround formats.
Pixel	Picture Element. Refers to the actual element of the picture and the data point in the digital video stream representing such an element. This term may also apply to the data that is carried across the HDMI link during a single TMDS (pixel) clock cycle, even if that data does not actually represent a picture element.
Pixel Encoding	Bit placement and sequencing for the components of a pixel for a particular color space and chroma sampling.
Root (Device)	A device, generally a display device, formally defined by the following rule: A device that has no HDMI output or, a device which has chosen to take the physical address 0.0.0.0.
Receiver	A component that is responsible for receiving the four differential TMDS input pairs at the input to an HDMI Sink and converting those signals into a digital output indicating a 24 bit, 12 bit, or 6 bit TMDS decoded word and indicating the TMDS coding mode used to decode those bits. This digital output may be contained within a semiconductor device or may be output from a semiconductor device.
Stereo	2 channel audio.
Stream	A time-ordered set of digital data originating from one Source and terminating at zero or more Sinks. A stream is characterized by bounded bandwidth requirements.
T_{bit}	Time duration of a single bit carried across the TMDS data channels.
T_{pixel}	Time duration of a single pixel carried across the TMDS data channels. This is equal to $10 * T_{bit}$.
Transmitter	A component that is responsible for driving the four differential TMDS output pairs into an HDMI output and for clocking the data driven into those four output pairs.
Video Field	The period from one VSYNC active edge to the next VSYNC active edge.
Video Format	A video format is sufficiently defined such that when it is received at the monitor, the monitor has enough information to properly display the video to the user. The definition of each format includes a Video Format Timing, the picture aspect ratio, and a colorimetry space.
Video Format Timing	The waveform associated with a video format. Note that a specific Video Format Timing may be associated with more than one Video Format (e.g., 720X480p@4:3 and 720X480p@16:9).
YC_BC_R	Digital representation of any video signal using one of several luminance/color-difference color spaces.

2.3 Acronyms and Abbreviations

ANSI	American National Standards Institute
AVI	Auxiliary Video Information
CEA	Consumer Electronics Association
CEC	Consumer Electronics Control
CTS	Cycle Time Stamp
DDC	Display Data Channel
DDWG	Digital Display Working Group
DTV	Digital Television
DVD	Digital Versatile Disc
DVI	Digital Visual Interface
E-DDC	Enhanced Display Data Channel
E-EDID	Enhanced Extended Display Identification Data
ECC	Error Correction Code
EDID	Extended Display Identification Data
EIA	Electronic Industries Alliance
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
HPD	Hot Plug Detect
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
ITU	International Telecommunications Union
L-PCM	Linear Pulse-Code Modulation
LSb	least significant bit
MPEG	Moving Picture Experts Group
MSb	most significant bit

N.C.	No connect.
PCB	Printed Circuit Board
Rx	Receiver
SMPTE	Society of Motion Picture & Television Engineers
STB	Set-Top Box
TERC4	TMDS Error Reduction Coding – 4 bit
TMDS	Transition Minimized Differential Signaling
Tx	Transmitter
VESA	Video Electronics Standards Association
VSDB	Vendor-Specific Data Block

3 Overview

HDMI system architecture is defined to consist of Sources and Sinks. A given device may have one or more HDMI inputs and one or more HDMI outputs. Each HDMI input on these devices shall follow all of the rules for an HDMI Sink and each HDMI output shall follow all of the rules for an HDMI Source.

As shown in *Figure 3-1 HDMI Block Diagram* the HDMI cable and connectors carry four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio and auxiliary data. In addition, HDMI carries a VESA DDC channel. The DDC is used for configuration and status exchange between a single Source and a single Sink. The optional CEC protocol provides high-level control functions between all of the various audiovisual products in a user's environment.

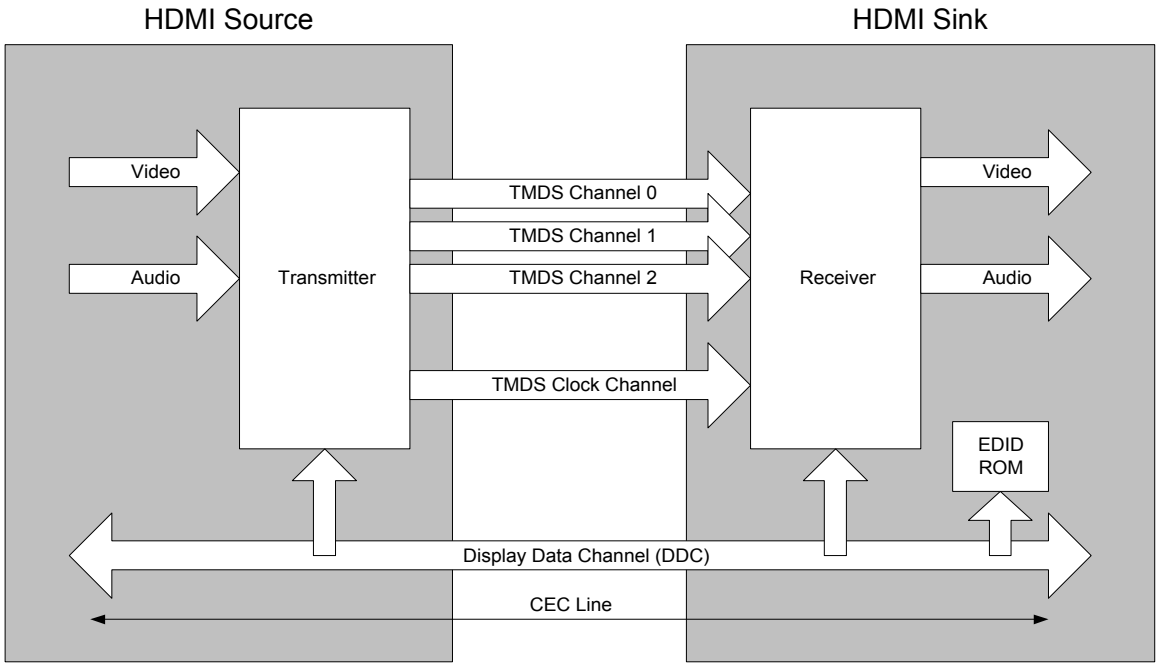

Figure 3-1 HDMI Block Diagram

Audio, video and auxiliary data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver as a frequency reference for data recovery on the three TMDS data channels.

Video data is carried as a series of 24-bit pixels on the three TMDS data channels. TMDS encoding converts the 8 bits per channel into the 10 bit DC-balanced, transition minimized sequence which is then transmitted serially across the pair at a rate of 10 bits per pixel clock period.

Video pixel rates can range from 25MHz to 165MHz. Video formats with rates below 25MHz (e.g. 13.5MHz for 480i/NTSC) can be transmitted using a pixel-repetition scheme. The video pixels can be encoded in either RGB, YC_BC_R 4:4:4 or YC_BC_R 4:2:2 formats. In all three cases, up to 24 bits per pixel can be transferred.

In order to transmit audio and auxiliary data across the TMDS channels, HDMI uses a packet structure. In order to attain the higher reliability required of audio and control data, this data is protected with a BCH error correction code and is encoded using a special error reduction coding to produce the 10-bit word that is transmitted.

Basic audio functionality consists of a single IEC 60958 audio stream at sample rates of 32kHz, 44.1kHz or 48kHz. This can accommodate any normal stereo stream. Optionally, HDMI can carry a single such stream at sample rates up to 192KHz or from two to four such streams (3 to 8 audio channels) at sample rates up to 96KHz. HDMI can also carry IEC 61937 compressed (e.g. surround-sound) stream at sample rates up to 192kHz.

The DDC is used by the Source to read the Sink's Enhanced Extended Display Identification Data (E-EDID) in order to discover the Sink's configuration and/or capabilities.

4 Physical Layer

4.1 Connectors and Cables

4.1.1 Overview of Connectors

A device's external HDMI connection shall be presented via one of the two specified HDMI connectors, Type A or Type B. This connector can be attached directly to the device or can be attached via a cable adapter that is shipped with the device.

The Type A connector carries all required HDMI signals, including a single TMDS link. The Type B connector is slightly larger and carries a second TMDS link, which is necessary to support very high-resolution computer displays requiring dual link bandwidth.

A passive cable adapter between Type A and Type B connectors is specified.

4.1.2 Connector Support Requirements

4.1.2.1 HDMI Sources

An HDMI Source connection using a Type A connector shall transmit only video format timings that are:

- Described in Section 6.3, or,
- Defined, per EDID Ver. 1.3, in the first, and only the first Detailed (18-byte) Timing Descriptor of a concurrently attached HDMI compliant Sink.

An HDMI Source connection using a Type B connector may transmit any video format timing.

4.1.2.2 HDMI Sinks

An HDMI Sink connection using a Type A connector may define support, via E-EDID, only for video format timings that are:

- Described in Section 6.3, or,
- Defined within the first and only the first Detailed (18-byte) Timing Descriptor found in the EDID 1.3 structure of this Sink.

An HDMI Sink connection using a Type B connector may define support for any video format timing, via any of the EDID 1.3 or EIA/CEA-861B mechanisms.

Beyond the specific video format timing restrictions defined in this section (above), no other video differences between Type A and Type B devices are defined in this specification.

4.1.3 Dual-Link

The Type A connector carries only a single TMDS link and is therefore only permitted to carry signals up to 165Mpixels/sec.

To support signals greater than 165Mpixels/sec, the dual-link capability of the Type B connector shall be used.

HDMI dual-link architecture is compatible with DVI 1.0 dual-link architecture and is defined in Appendix B.

4.1.4 Connector Drawings

All dimensions in millimeters.

4.1.4.1 Type A Receptacle

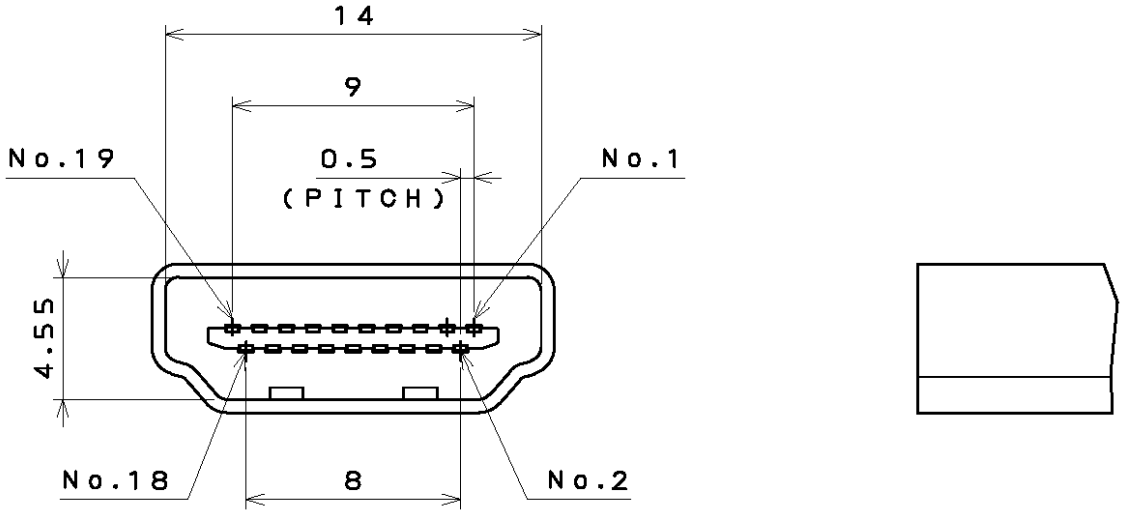

Figure 4-1 Type A Receptacle

4.1.4.2 Type A Plug

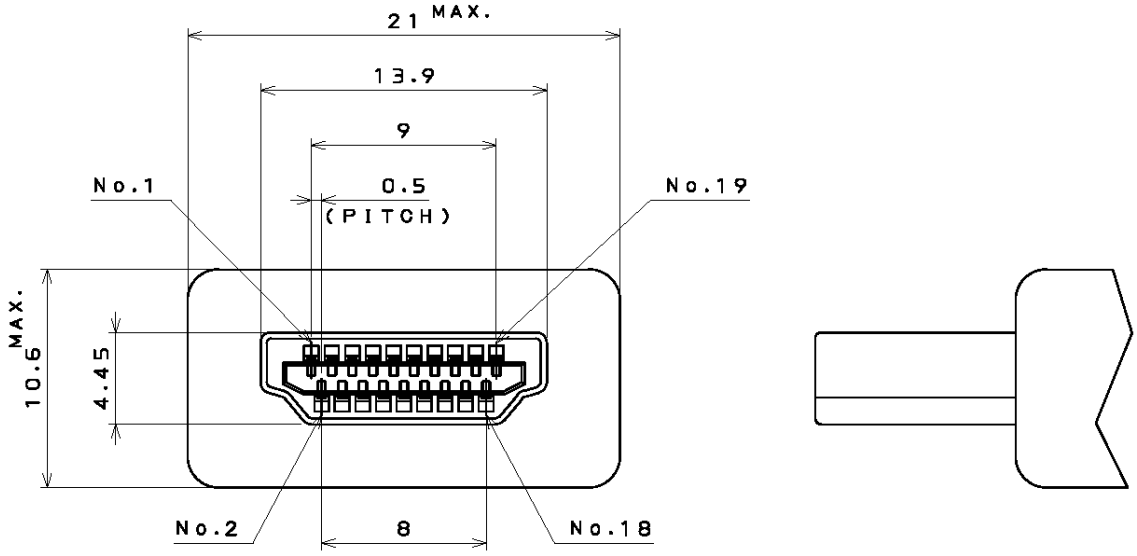

Figure 4-2 Type A Plug Mating Interface Dimensions

4.1.4.3 Type B Receptacle

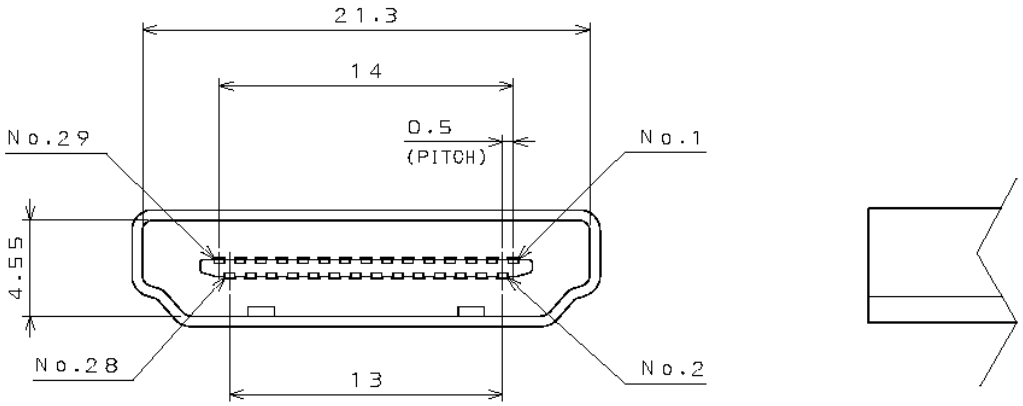

Figure 4-3 Type B Receptacle

4.1.4.4 Type B Plug

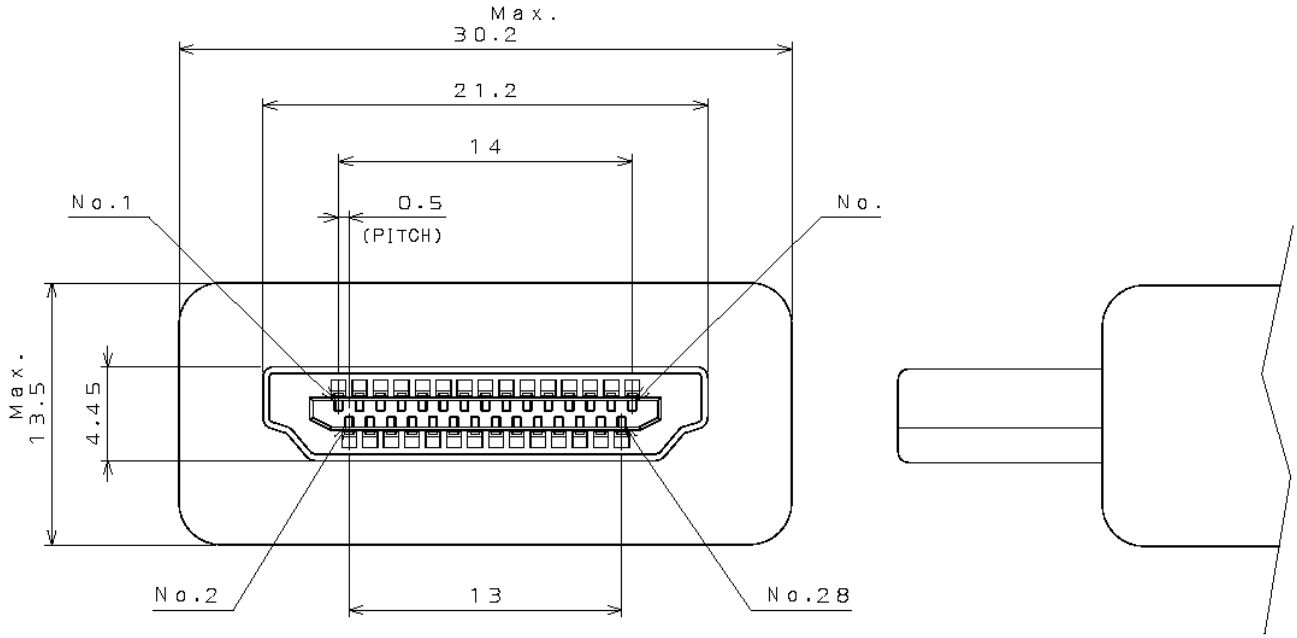

Figure 4-4 Type B Plug Mating Interface Dimensions

5 Signaling And Encoding

5.1 Overview

5.1.1 Link Architecture

As shown in Figure 5-1, an HDMI link includes three TMDS Data channels and a single TMDS Clock channel. The TMDS Clock channel constantly runs at the pixel rate of the transmitted video. During every cycle of the TMDS Clock channel, each of the three TMDS data channels transmits a 10-bit character. This 10-bit word is encoded using one of several different coding techniques.

The input stream to the Source's encoding logic will contain video pixel, packet and control data. The packet data consists of audio and auxiliary data and associated error correction codes.

These data items are processed in a variety of ways and are presented to the TMDS encoder as either 2 bits of control data, 4 bits of packet data or 8 bits of video data per TMDS channel. The Source encodes one of these data types or encodes a Guard Band character on any given clock cycle.

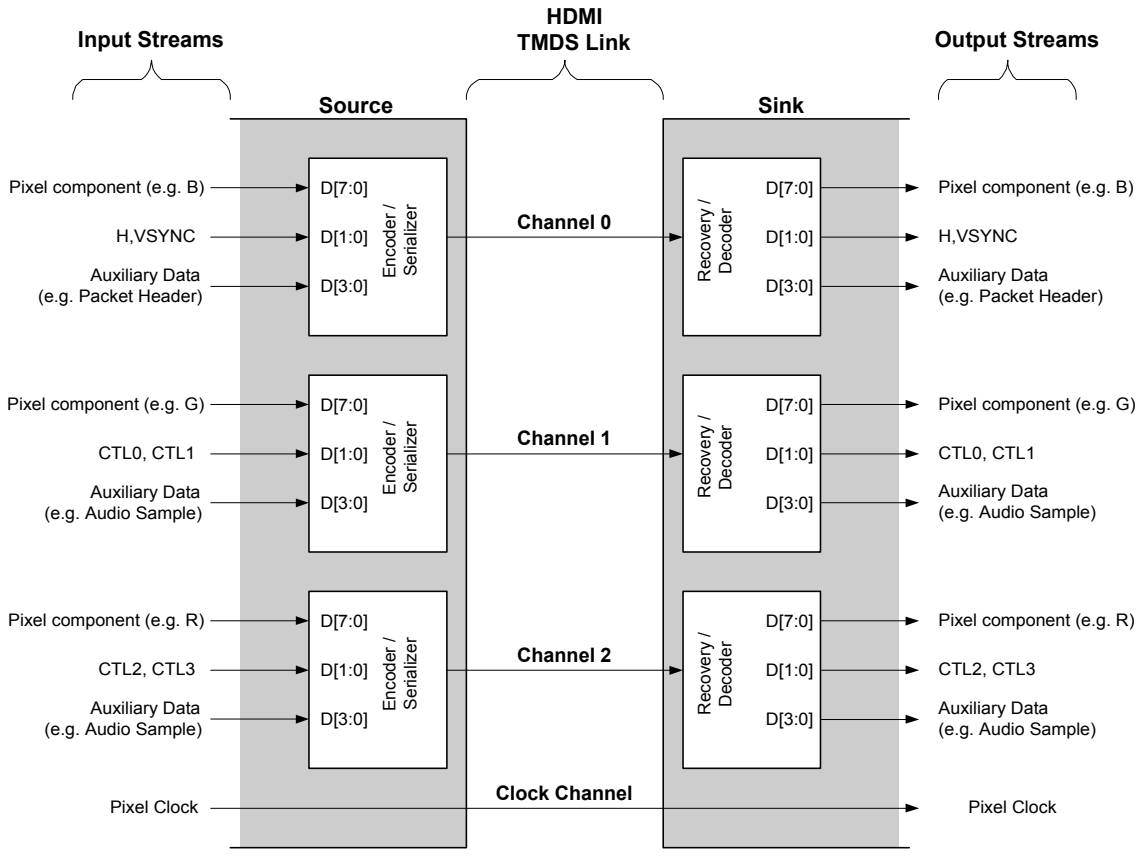

Figure 5-1 HDMI Encoder/Decoder Overview

5.1.2 Operating Modes Overview

The HDMI link operates in one of three modes: Video Data Period, Data Island period, and Control period. During the Video Data Period, the active pixels of an active video line are transmitted. During the Data Island period, audio and auxiliary data are transmitted using a series of packets. The Control period is used when no video, audio, or auxiliary data needs to be transmitted. A Control Period is required between any other two periods.

An example of each period placement is shown in the following figure.

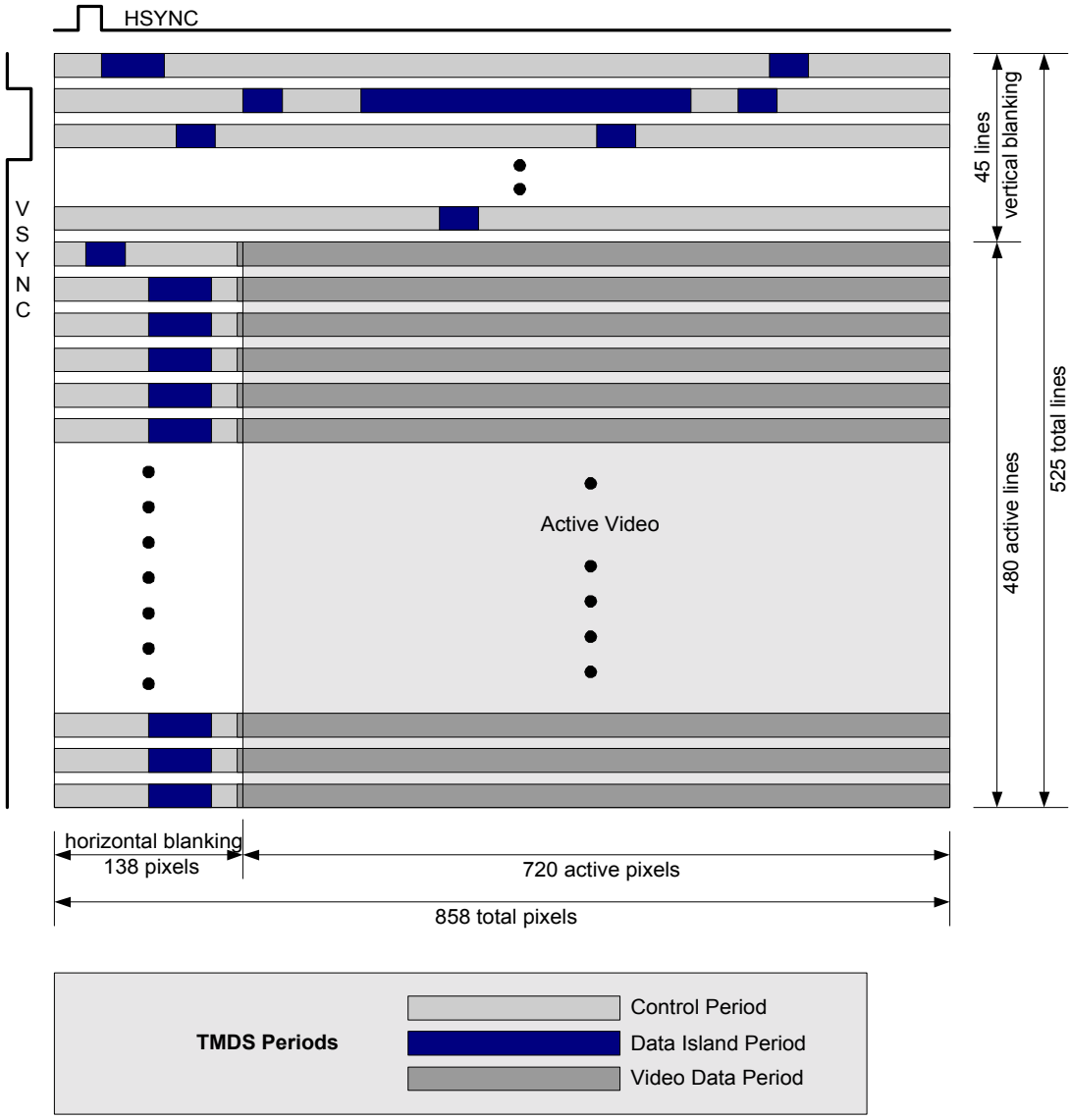

Figure 5-2 Informative Example: TMDS periods in 720x480p video frame

Video Data Periods use transition minimized coding to encode 8 bits per channel, or 24 bits total per pixel.

Data Island Periods are encoded using a similar transition minimized coding, TMDS Error Reduction Coding (TERC4), which transmits 4 bits per channel, or 12 bits total per pixel clock period.

During Control Periods, 2 bits per channel, or 6 bits total are encoded per pixel clock using a transition maximized encoding. These 6 bits are HSYNC, VSYNC, CTL0, CTL1, CTL2 and CTL3. Near the end of every Control Period, a Preamble, using the CTLx bits, indicates whether the next Data Period is a Video Data Period or a Data Island Period.

Each Video Data Period and Data Island Period starts with a Leading Guard Band designed to provide robust determination of the transition from the Control Period to the Data Period. This Leading Guard Band consists of two special characters.

The Data Island Period is also protected by a Trailing Guard Band, which is designed to provide a robust determination of the transition to Control Period.

The following table shows Encoding type used and data transmitted during each operating mode.

Table 5-1 Encoding Type and Data Transmitted

Period	Data Transmitted	Encoding Type
Video Data	Video Pixels	Video Data Coding (8 bits converted to 10 bits)
	(Guard Band)	(Fixed 10 bit pattern)
Data Island	Packet Data - Audio Samples - InfoFrames HSYNC, VSYNC	TERC4 Coding (4 bits converted to 10 bits)
	(Guard Band)	(Fixed 10 bit pattern)
Control	Control - Preamble - HSYNC, VSYNC	Control Period Coding (2 bits converted to 10 bits)

Table 5-2 shows the available packet types.

Table 5-2 Packet Types

Packet Type Value	Packet Type
0x00	Null
0x01	Audio Clock Regeneration (N/CTS)
0x02	Audio Sample
0x03	General Control
0x80+InfoFrame Type	EIA/CEA-861B InfoFrame

6 Video

6.1 Overview

HDMI allows a wide variety of explicitly defined video format timings to be transmitted and displayed. These video format timings define the pixel and line counts and timing, synchronization pulse position and duration, and whether the format is interlaced or progressive.

The video pixels carried across the link shall be in one of three different pixel encodings: RGB 4:4:4, YC_BC_R 4:4:4 or YC_BC_R 4:2:2.

The HDMI Source determines the pixel encoding and video format of the transmitted signal based on the characteristics of the source video, the format and pixel encoding conversions possible at the Source, and the format and pixel encoding capabilities and preferences of the Sink.

6.2 Video Format Support

In order to provide maximum compatibility between video Sources and Sinks, specific minimum requirements have been specified for Sources and Sinks.

6.2.1 Format Support Requirements

Some of the following support requirements are in addition to those specified in EIA/CEA-861B.

- An HDMI Source shall support at least one of the following video format timings:
  - 640x480p @ 59.94/60Hz
  - 720x480p @ 59.94/60Hz
  - 720x576p @ 50Hz
- An HDMI Source that is capable of transmitting any of the following video format timings using any other component analog or uncompressed digital video output, shall be capable of transmitting that video format timing across the HDMI interface.
  - 1280x720p @ 59.94/60Hz
  - 1920x1080i @ 59.94/60Hz
  - 720x480p @ 59.94/60Hz
  - 1280x720p @ 50Hz
  - 1920x1080i @ 50Hz
  - 720x576p @ 50Hz
- An HDMI Sink which accepts 60Hz video formats shall support the 640x480p @ 59.94/60Hz and 720x480p @ 59.94/60Hz video format timings.
- An HDMI Sink which accepts 50Hz video formats shall support the 640x480p @ 59.94/60Hz and 720x576p @ 50Hz video format timings.
- An HDMI Sink which accepts 60Hz video formats, and which supports HDTV capability, shall support 1280x720p @ 59.94/60Hz or 1920x1080i @ 59.94/60Hz video format timings.
- An HDMI Sink which accepts 50Hz video formats, and which supports HDTV capability, shall support 1280x720p @ 50Hz or 1920x1080i @ 50Hz video format timings.

- An HDMI Sink that is capable of receiving any of the following video format timings using any other component analog or uncompressed digital video input, shall be capable of receiving that format across the HDMI interface.
  - 1280x720p @ 59.94/60Hz
  - 1920x1080i @ 59.94/60Hz
  - 1280x720p @ 50Hz
  - 1920x1080i @ 50Hz

6.2.2 Video Control Signals : HSYNC, VSYNC

During the Data Island period, HDMI carries HSYNC and VSYNC signals using encoded bits on Channel 0. During Video Data periods, HDMI does not carry HSYNC and VSYNC and the Sink should assume that these signals remain constant. During Control periods, HDMI carries HSYNC and VSYNC signals through the use of four different control characters on TMDS Channel 0.

6.2.3 Pixel Encoding Requirements

Only pixel encodings of RGB 4:4:4, YC_BC_R 4:2:2, and YC_BC_R 4:4:4 (as specified in Section 6.5) may be used on HDMI.

All HDMI Sources and Sinks shall be capable of supporting RGB 4:4:4 pixel encoding.

All HDMI Sources shall support either YC_BC_R 4:2:2 or YC_BC_R 4:4:4 pixel encoding whenever that device is capable of transmitting a color-difference color space across any other component analog or digital video interface.

All HDMI Sinks shall be capable of supporting both YC_BC_R 4:4:4 and YC_BC_R 4:2:2 pixel encoding when that device is capable of supporting a color-difference color space from any other component analog or digital video input.

If an HDMI Sink supports either YC_BC_R 4:2:2 or YC_BC_R 4:4:4 then both shall be supported.

An HDMI Source may determine the pixel-encodings that are supported by the Sink through the use of the E-EDID. If the Sink indicates that it supports YC_BC_R-formatted video data and if the Source can deliver YC_BC_R data, then it can enable the transfer of this data across the link.

6.3 Video Format Timing Specifications

All specified video line pixel counts and video field line counts (both active and total) and HSYNC and VSYNC positions and durations shall be adhered to when transmitting a specified video format timing.

For example, if a Source is processing material with fewer active pixels per line than required (i.e. 704 pixels vs. 720 pixels for standard definition MPEG2 material), it may add pixels to the left and right of the supplied material before transmitting across HDMI. AVI bar info may need to be adjusted to account for these added pixels.

Detailed timing is found in EIA/CEA-861B for the following primary and optional video format timings.

6.3.1 Primary Video Format Timings

- 640x480p @ 59.94/60Hz
- 1280x720p @ 59.94/60Hz
- 1920x1080i @ 59.94/60Hz
- 720x480p @ 59.94/60Hz
- 720(1440)x480i @ 59.94/60Hz
- 1280x720p @ 50Hz
- 1920x1080i @ 50Hz
- 720x576p @ 50Hz
- 720(1440)x576i @ 50Hz

6.3.2 Optional Video Format Timings

- 720(1440)x240p @ 59.94/60Hz
- 2880x480i @ 59.94/60Hz
- 2880x240p @ 59.94/60Hz
- 1440x480p @ 59.94/60Hz
- 1920x1080p @ 59.94/60Hz
- 720(1440)x288p @ 50Hz
- 2880x576i @ 50Hz
- 2880x288p @ 50Hz
- 1440x576p @ 50Hz
- 1920x1080p @ 50Hz
- 1920x1080p @ 23.98/24Hz
- 1920x1080p @ 25Hz
- 1920x1080p @ 29.97/30Hz

6.4 Pixel-Repetition

Video formats with native pixel rates below 25 Mpixels/sec require pixel-repetition in order to be carried across a TMDS link. 720x480i and 720x576i video format timings shall always be pixel-repeated.

The HDMI Source indicates the use of pixel-repetition with the Pixel Repetition (PR0:PR3) field in the AVI InfoFrame. This field indicates to the HDMI Sink how many repetitions of each unique pixel are transmitted. In non-repeated formats, this value is zero.

For pixel-repeated formats, this value indicates the number of pixels that may be discarded by the Sink without losing real image content.

The Source shall always accurately indicate the pixel repetition count being used. The use of the Pixel Repetition field is optional for HDMI Sink.

The use of this pixel-repetition count field is more fully described in EIA/CEA-861B.

6.5 Pixel Encodings

There are three different pixel encodings that may be sent across an HDMI cable: YC_BC_R 4:4:4, YC_BC_R 4:2:2 and RGB 4:4:4. Whichever encoding is used, it shall conform to one of the methods described in this section.

Figure 6-1 shows the default encoding, RGB 4:4:4. The R, G, and B components of the first pixel for a given line of video are transferred on the first pixel of the video data period following the Guard Band characters.

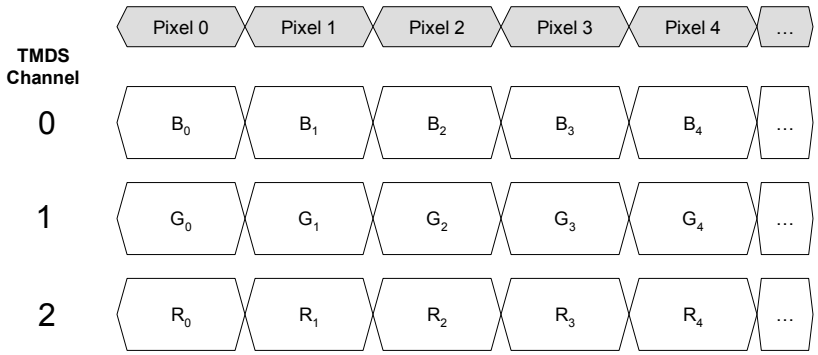

Figure 6-1 Default pixel encoding: RGB 4:4:4, 8 bits/component

Figure 6-2 shows the signal mapping and timing for transferring YC_BC_R 4:2:2 data across HDMI. Because 4:2:2 data only requires two components per pixel clock, more bits are allocated per component. The available 24 bits are split into 12 bits for the Y component and 12 bits for the C components.

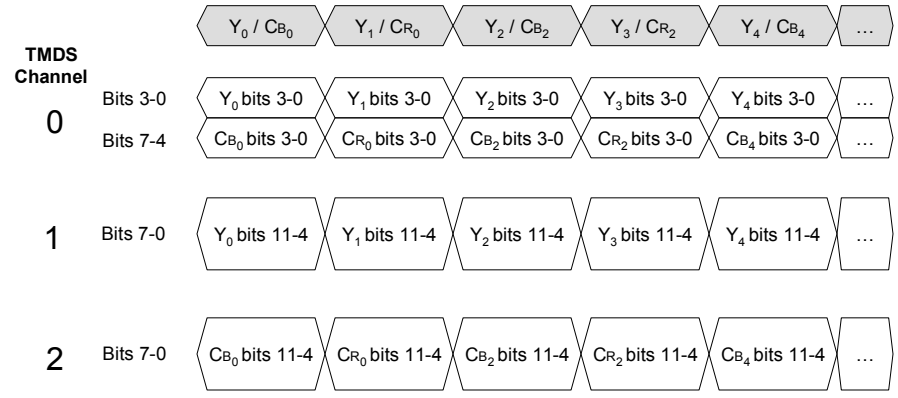

Figure 6-2 YC_BC_R 4:2:2 component

The YC_BC_R 4:2:2 pixel encoding on HDMI closely resembles standard ITU-R BT.601. The high-order 8 bits of the Y samples are mapped onto the 8 bits of Channel 1 and the low-order 4 bits

are mapped onto the low-order 4 bits of Channel 0. If fewer than 12 bits are used, the valid bits shall be left-justified (i.e. MSb=MSb) with zeroes padding the bits below the LSb.

The first pixel transmitted within a Video Data Period contains three components, Y0, Cb0 and Cr0. The Y0 and Cb0 components are transmitted during the first TMDS pixel clock period while Cr0 is transmitted during the second TMDS pixel clock period. This second pixel clock period also contains the only component for the second pixel – Y1. In this way, the link carries one C_B sample for every two TMDS pixel clocks and one Cr sample for every two TMDS pixel clocks. These two components (C_B and C_R) are multiplexed onto the same signal paths on the link.

At the third TMDS pixel clock, this process is repeated with the Y and C_B components for the third pixel being transmitted, followed, on the next clock, by the C_R component of the third pixel and the Y component of the fourth pixel.

YC_BC_R 4:4:4 data is transferred using the scheme illustrated in Figure 6-3.

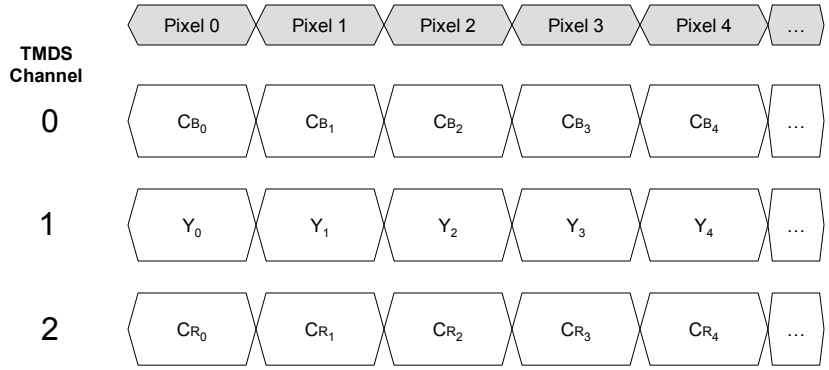

Figure 6-3 8-bit YC_BC_R 4:4:4 mapping

During pixel-doubling (Pixel_Repetition_Count = 1), all of the data sent across during the first pixel clock will be repeated during the second pixel clock. The third clock will then represent the second actual pixel and so on.

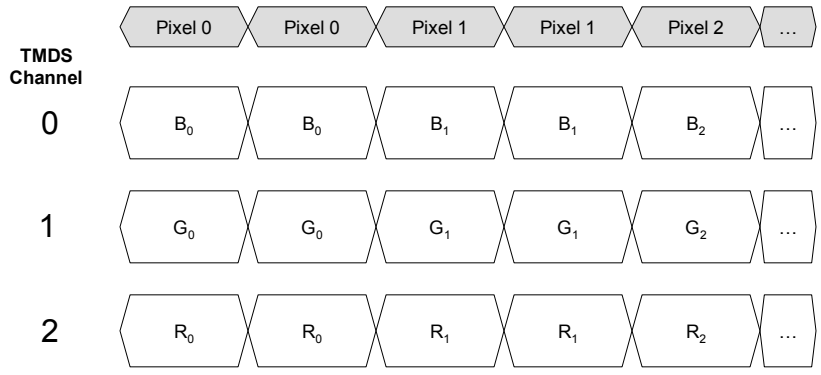

Figure 6-4 RGB with Pixel-Doubling

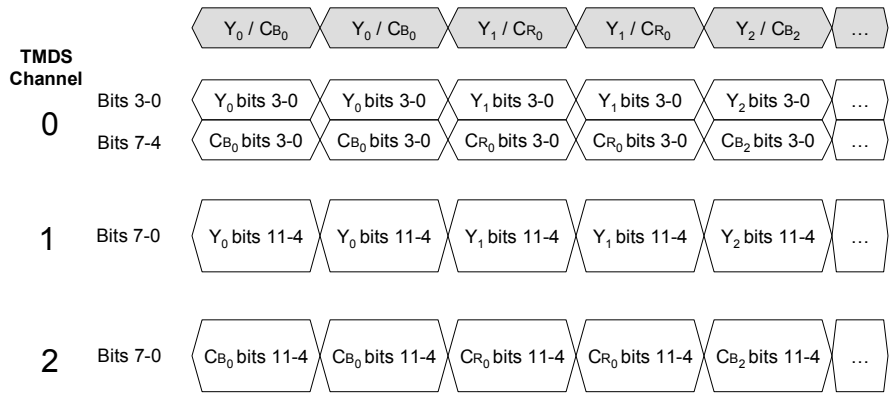

Figure 6-5 YC_BC_R 4:2:2 with Pixel-Doubling

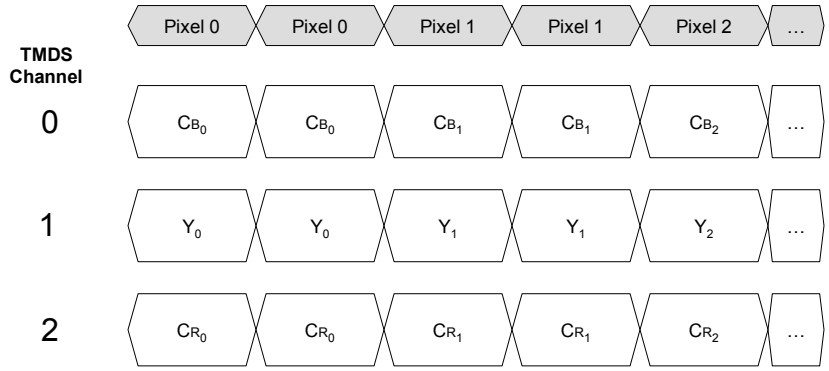

Figure 6-6 YC_BC_R 4:4:4 with Pixel-Doubling

6.6 Video Quantization Ranges

Black and white levels for video components shall be either “Full Range” or “Limited Range.” YC_BC_R components shall always be Limited Range while RGB components may be either Full Range or Limited Range. While using RGB, Limited Range shall be used for all video formats defined in EIA/CEA-861B, with the exception of VGA (640x480) format which requires Full Range.

Table 6-1 Video Color Component Ranges

Color Space	Component Bit Depth	for Full range		for Limited range	
		Black level	White level	Black level	White level
R / G / B	8	0	255	16	235
Y / C_B / C_R	8	not allowed		16	235 (Y), 240 (C_B, C_R)
Y / C_B / C_R	10	not allowed		64	940 (Y), 960 (C_B, C_R)
Y / C_B / C_R	12	not allowed		256	3760 (Y), 3840 (C_B, C_R)

6.7 Colorimetry

6.7.1 480p, 480i, 576p, 576i, 240p and 288p

The 480-line, 576-line, 240-line, and 288-line video formats are typically transmitted with a color space based on SMPTE 170M.

ITU-R BT.601-5 Section 3.3 shall be used for any color space conversion needed in the course of processing unless a different colorimetry is specified in the AVI InfoFrame.

The encoding parameter values shall be as defined in Table 3 of ITU-R BT.601-5 and as summarized in Section 6.6.

6.7.2 1080i, 1080p and 720p

The high-definition video formats are typically transmitted with a color space based on ITU-R BT.709-4.

ITU-R BT.709-4 Part 1, Section 4 shall be used for any color space conversion needed in the course of processing unless a different colorimetry is specified in the AVI InfoFrame.

The digital representation shall be as defined in Part 1, Section 6.10 of ITU-R BT.709-4 and as summarized in Section 6.6.

7 Audio

7.1 Relationship with IEC 60958/IEC 61937 (IEC)

Audio data is formatted in the Audio Sample Packet as a structure that closely resembles an IEC 60958 or IEC 61937 frame.

On HDMI, each IEC 60958 sub-frame is represented as a 28-bit word. There is no encoding of the preamble type, which instead is replaced with a “B” bit (start-of-block) in each Audio Sample packet. The B bit shall be set for a “B, W” frame and shall be clear for an “M, W” frame. (IEC 60958-1 Section 4.1.2). No other sub-frame preamble combinations are allowed.

Except where specifically indicated in this document, the behavior of all fields within the Audio Sample Subpackets shall follow the corresponding rules specified in the IEC 60958 or IEC 61937 specifications.

With the exception of the Channel Number field carried within the IEC 60958 Channel Status block, the corresponding Channel Status bits for all of the transmitted channels shall be identical.

7.2 Audio Sample Clock Capture and Regeneration

Audio data being carried across the HDMI link, which is driven by a TMDS (video) clock only, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.

There are a variety of clock regeneration methods that can be implemented in an HDMI Sink, each with a different set of performance characteristics. This specification does not attempt to define exactly how these mechanisms operate. It does however present a possible configuration and it does define the data items that the HDMI Source shall supply to the HDMI Sink in order to allow the HDMI Sink to adequately regenerate the audio clock. It also defines how that data shall be generated.

In many video source devices, the audio and video clocks are generated from a common clock (coherent clocks). In this situation, there exists a rational (integer divided by integer) relationship between these two clocks. The HDMI clock regeneration architecture can take advantage of this rational relationship and can also work in an environment where there is no such relationship between these two clocks, that is, where the two clocks are truly asynchronous or where their relationship is unknown.

Figure 7-1 Audio Clock Regeneration model, illustrates the overall system architecture model used by HDMI for audio clock regeneration. The Source shall determine the fractional relationship between the video clock and an audio reference clock (128 * audio sample rate) and shall pass the numerator and denominator for that fraction to the Sink across the HDMI link. The Sink may then recreate the audio clock from the TMDS clock by using a clock divider and a clock multiplier.

The exact relationship between the two clocks will be:

$$128 * f_S = f_{TMDS\_clock} * N / CTS.$$

The Source shall determine the value of the numerator N. Typically, this value N will be used in a clock divider to generate an intermediate clock that is slower than the $128 * f_S$ clock by the factor N. The Source will typically determine the value of the denominator CTS (Cycle Time Stamp) by counting the number of TMDS clocks in each of the $128 * f_S/N$ clocks.

If there is a constant fractional relationship between these two clocks, and the two clocks are exactly synchronous, then the CTS value will quickly come to a constant value. If the clocks are asynchronous, or there is some amount of jitter between the two clocks, then the CTS value will typically alternate between two or three different values. Greater variations are possible with larger jitter.

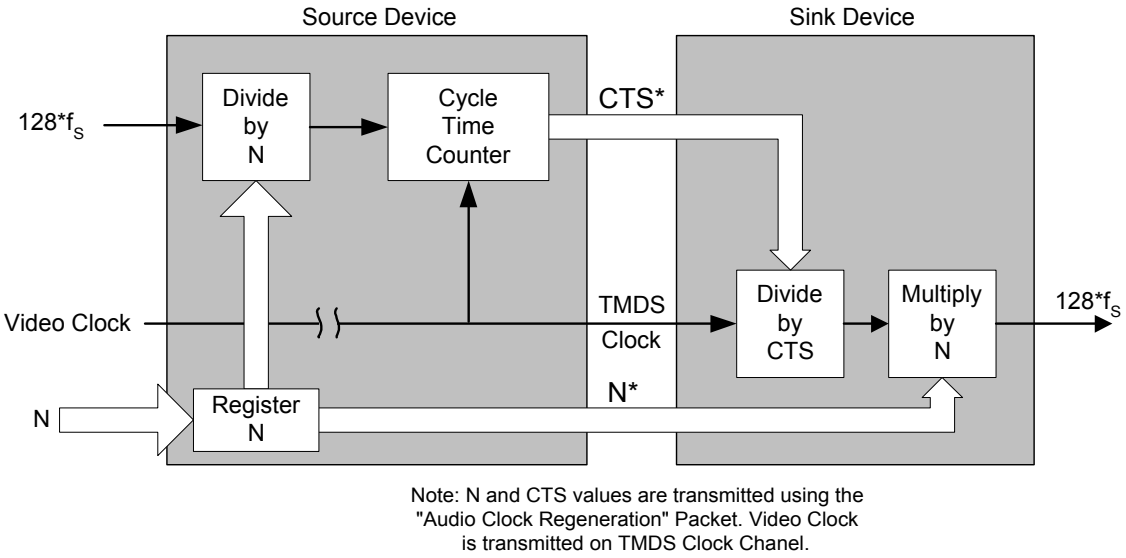

Figure 7-1 Audio Clock Regeneration model

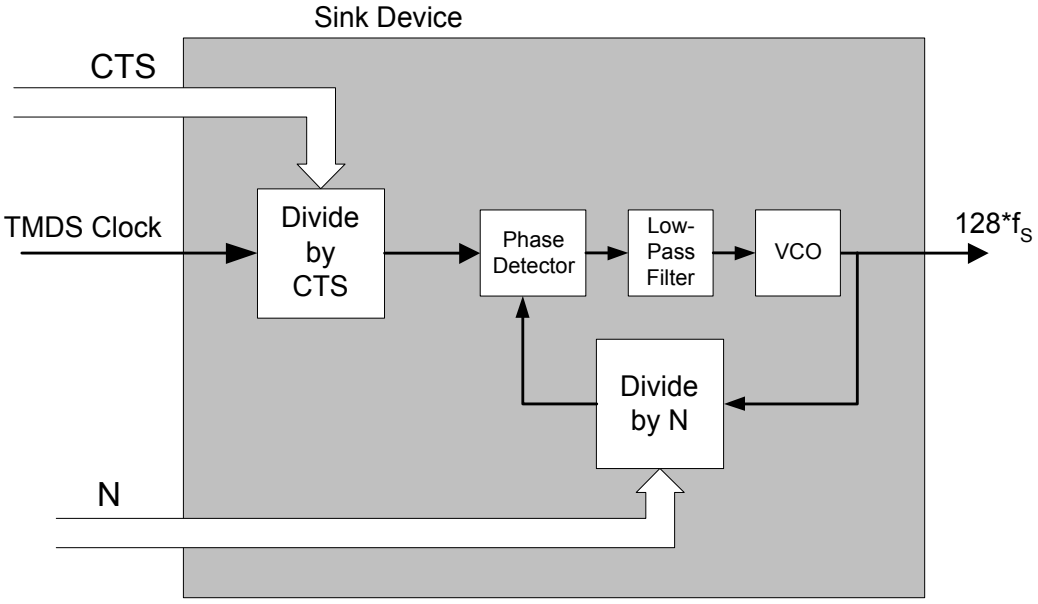

Figure 7-2 Optional Implementation: Audio Sink

It is expected that most Sinks will be implemented with an architecture similar to that shown in Figure 7-2, however, it is permitted and possible to devise an audio clock regeneration function that does not take advantage of the N or CTS values passed to the Sink.

7.3 Audio Sample Rates and Support Requirements

If an HDMI Source supports audio transmission across any output, then it shall support HDMI audio transmission. Exceptions to this rule for Sources with Type B connectors are found in Appendix B.

If an HDMI Source supports any HDMI audio transmission, then it shall support 2 channel L-PCM using an IEC 60958 Subpacket structure, with either 32kHz, 44.1kHz or 48kHz sampling rate and a sample size of 16 bits or more.

An HDMI Source is permitted to transmit L-PCM or encoded audio data at sample rates of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz using either IEC 60958 format or IEC 61937 format.

If an HDMI Sink supports audio reception across any input, then it shall support audio reception from all HDMI inputs.

An HDMI Sink that is capable of accepting any audio format is required to accept two channel IEC 60958-formatted L-PCM audio at sample rates of 32kHz, 44.1kHz, and 48kHz.

For EIA/CEA-861B references to Sources, “Basic Audio” is defined as two channel L-PCM audio at sample rates of 32kHz, 44.1kHz, *or* 48kHz, with a sample size of at least 16 bits. For EIA/CEA-861B references to DTV devices, “Basic Audio” is defined as two channel L-PCM audio at sample rates of 32kHz, 44.1kHz, *and* 48kHz. There is no sample size usage restriction for DTV devices.

An HDMI Sink may optionally accept audio at sample rates of 88.2kHz, 96kHz, 176.4kHz and/or 192kHz using either IEC 60958 format or IEC 61937 format, and should indicate these capabilities in the E-EDID data structure.

An HDMI Repeater shall support HDMI audio reception and transmission.

Whenever transmitting a valid audio stream, HDMI Sources shall always include valid sample rate information in the Channel Status bits of the audio sample packets, per Table 7-1.

In some cases, pixel-repetition may be required to increase the available bandwidth for audio transmission. For instance, when transmitting a 720x480p video format timing, it is required to pixel double in order to transmit 6 channels @ 96kHz.

Table 7-1 Channel Status Values for Audio Sample Frequencies

Channel Status Bit Number				Sample Frequency
24	25	26	27	
1	1	0	0	32 kHz
0	0	0	0	44.1 kHz
0	0	0	1	88.2 kHz
0	0	1	1	176.4 kHz
0	1	0	0	48 kHz
0	1	0	1	96 kHz
0	1	1	1	192 kHz

7.3.1 Video Dependency

Available audio bandwidth depends upon the pixel clock frequency, the video format timing, and whether or not content protection re-synchronization is needed.

Table 7-2 shows the available audio sample rates for 2-channel (Layout 0) and 8-channel (Layout 1) audio transmission at the various video format timings specified in EIA/CEA-861B, assuming that 58 clocks of the horizontal blanking interval is required for content protection re-synchronization.

Table 7-2 Maximum Audio Sampling Frequency for all Video Format Timings (Informative)

Description	Format Timing	Pixel Repetition	Vertical Freq (Hz)	Max f_S 8 ch (kHz)	Max f_S 2 ch (kHz)
60Hz Formats					
VGA	640x480p	none	59.94/60	48	192
480i	1440x480i	2	59.94/60	48	192
480i	2880x480i	4	59.94/60	192	192
240p	1440x240p	2	59.94/60	48	192
240p	2880x240p	4	59.94/60	192	192
480p	720x480p	none	59.94/60	48	192
480p	1440x480p	2	59.94/60	96	192
720p	1280x720p	none	59.94/60	192	192
1080i	1920x1080i	none	59.94/60	192	192
1080p	1920x1080p	none	59.94/60	192	192
50Hz Formats					
576i	1440x576i	2	50	48	192
576i	2880x576i	4	50	192	192
288p	1440x288p	2	50	48	192
288p	2880x288p	4	50	192	192
576p	720x576p	none	50	48	192
576p	1440x576p	2	50	96	192
720p/50	1280x720p	none	50	192	192
1080i/50	1920x1080i	none	50	192	192
1080p/50	1920x1080p	none	50	192	192
1080p @ 24-30Hz					
1080p	1920x1080p	none	24	192	192
1080p	1920x1080p	none	25	192	192
1080p	1920x1080p	none	29.97/30	192	192

7.4 Channel / Speaker Assignment

HDMI allows a Sink to indicate the configuration of attached speakers through the use of the Speaker Allocation Data Block described in EIA/CEA-861B page 84 and Table 36.

In addition, for multi-channel L-PCM audio streams, the Source may specify the speaker assignment for each of the channels in the audio stream delivered to the Sink. EIA/CEA-861B Section 6.3.2 specifies the available speaker assignments for active audio channels on HDMI. The indication of the current speaker assignment is carried in the Audio InfoFrame.

7.5 Audio, Video Synchronization

For a variety of reasons, an HDMI link may add a delay to the audio and/or video.

An HDMI Source is required to transmit audio and video data streams with no more than ±2 msec of audio delay relative to the video. Due to the uneven transmission of audio data, the delay shall be considered to be the average delay of all of the audio sample packets over the course of 3 steady-state video frames.

8 Control And Configuration

8.1 Overview

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC.

TMDS is used to carry all audio and video data as well as auxiliary data, including AVI and Audio InfoFrames that describe the active audio and video streams.

The DDC channel is used by an HDMI Source to determine the capabilities and characteristics of the Sink by reading the E-EDID data structure.

HDMI Sources are expected to read the Sink's E-EDID and to deliver only the audio and video formats which are supported by the Sink. Also, HDMI Sinks are expected to detect InfoFrames and to process the received audio and video data appropriately.

The CEC channel is optionally used for higher-level user functions such as automatic setup tasks or tasks typically associated with infrared remote control usage.

8.2 EIA/CEA-861B InfoFrames

An InfoFrame packet carries one InfoFrame. The InfoFrame provided by HDMI is limited to 30 bytes plus a checksum byte. HDMI Sources are recommended to use the AVI InfoFrame and Audio InfoFrame. Other InfoFrames specified in EIA/CEA-861B are optional.

All InfoFrames are described in detail in EIA/CEA-861B Section 6. The following describes how two of these InfoFrames are placed within the InfoFrame Packet structure and any areas where HDMI behavior is different than that specified in EIA/CEA-861B.

8.2.1 Auxiliary Video information (AVI) InfoFrame

Various aspects of the current video stream are indicated by the HDMI Source to the Sink with an Auxiliary Video information (AVI) InfoFrame.

The packetization of the AVI InfoFrame Version 2 is shown below.

Table 8-1 AVI InfoFrame Packet Header

Byte \ Bit #	7	6	5	4	3	2	1	0
HB0	Packet Type = 0x82							
HB1	Version = 0x02							
HB2	0	0	0	Length = 13 (0x0D)				

Table 8-2 AVI InfoFrame Packet Contents

Packet Byte #	EIA/CEA-861B Byte #	7	6	5	4	3	2	1	0
PB0	N. A.	Checksum							
PB1	Data Byte 1	Rsvd (0)	Y1	Y0	A0	B1	B0	S1	S0
PB2	Data Byte 2	C1	C0	M1	M0	R3	R2	R1	R0
PB3	Data Byte 3	Reserved (0)						SC1	SC0
PB4	Data Byte 4	Rsvd (0)	VIC6	VIC5	VIC4	VIC3	VIC2	VIC1	VIC0
PB5	Data Byte 5	Reserved (0)				PR3	PR2	PR1	PR0
PB6	Data Byte 6	Line Number of End of Top Bar (lower 8 bits)							
PB7	Data Byte 7	Line Number of End of Top Bar (upper 8 bits)							
PB8	Data Byte 8	Line Number of start of Bottom Bar (lower 8 bits)							
PB9	Data Byte 9	Line Number of start of Bottom Bar (upper 8 bits)							
PB10	Data Byte 10	Pixel Number of End of Left Bar (lower 8 bits)							
PB11	Data Byte 11	Pixel Number of End of Left Bar (upper 8 bits)							
PB12	Data Byte 12	Pixel Number of End of Right Bar (lower 8 bits)							
PB13	Data Byte 13	Pixel Number of End of Right Bar (upper 8 bits)							
PB14-PB27	Data Bytes 14-27	Reserved (0)							

- Y0, Y1 RGB or YC_BC_R indicator. See EIA/CEA-861B table 8 for details.
- A0 Active Information Present. See EIA/CEA-861B table 8 for details.
- B0, B1 Bar Info data valid. See EIA/CEA-861B table 8 for details.
- S0, S1 Scan Information (i.e. overscan, underscan). See EIA/CEA-861B table 8 for details.
- C0, C1 Colorimetry (ITU BT.601, BT.709 etc.). See EIA/CEA-861B table 9 for details.
- M0, M1 Picture Aspect Ratio (4:3, 16:9). See EIA/CEA-861B table 9 for details.
- R0…R3 Active Format Aspect Ratio. See EIA/CEA-861B table 10 and Annex H for details.
- VIC0…VIC6 Video Format Identification Code. See EIA/CEA-861B table 13 for details.
- PR0…PR3 Pixel Repetition factor. See EIA/CEA-861B table 14 for details.
- SC1, SC0 Non-uniform Picture Scaling. See EIA/CEA-861B table 11 and paragraph on page 58.

Table 8-3 HDMI Valid Pixel Repeat Values for Each Format

Video Code	Video Description	EIA/CEA-861B Pixel Repeat Values	HDMI Pixel Repeat Values
1	640x480p @ 60Hz	No Repetition	No Repetition
2,3	720x480p @ 59.94/60Hz	No Repetition	No Repetition
4	1280x720p @ 59.94/60Hz	No Repetition	No Repetition
5	1920x1080i @ 59.94/60Hz	No Repetition	No Repetition
6,7	720(1440)x480i @ 59.94/60Hz	Pixel sent 2 times	Pixel sent 2 times
8,9	720(1440)x240p @ 59.94/60Hz	Pixel sent 2 times	Pixel sent 2 times
10,11	2880x480i @ 59.94/60Hz	Pixel sent 1 to 10 times	Pixel sent 1 to 10 times
12,13	2880x240p @ 59.94/60Hz	Pixel sent 1 to 10 times	Pixel sent 1 to 10 times
14,15	1440x480p @ 59.94/60Hz	No Repetition	Pixel sent 1 to 2 times**
16	1920x1080p @ 59.94/60Hz	No Repetition	No Repetition
17,18	720x576p @ 50Hz	No Repetition	No Repetition
19	1280x720p @ 50Hz	No Repetition	No Repetition
20	1920x1080i @ 50Hz	No Repetition	No Repetition
21,22	720(1440)x576i @ 50Hz	Pixel sent 2 times	Pixel sent 2 times
23,24	720(1440)x288p @ 50Hz	Pixel sent 2 times	Pixel sent 2 times
25,26	2880x576i @ 50Hz	Pixel sent 1 to 10 times	Pixel sent 1 to 10 times
27,28	2880x288 @ 50Hz	Pixel sent 1 to 10 times	Pixel sent 1 to 10 times
29,30	1440x576p @ 50Hz	No Repetition	Pixel sent 1 to 2 times**
31	1920x1080p @ 50Hz	No Repetition	No Repetition
32	1920x1080p @ 23.97/24Hz	No Repetition	No Repetition
33	1920x1080p @ 25Hz	No Repetition	No Repetition
34	1920x1080p @ 29.97/30Hz	No Repetition	No Repetition

** - Denotes change from EIA/CEA-861B valid values. Pixel repetition is required to support some audio formats at 720x480p and 720x576p video format timings. See Section 7.3.1

8.2.2 Audio InfoFrame

A Source shall indicate characteristics of the active audio stream through the use of the IEC 60958 Channel Status bits and through the use of the Audio InfoFrame. Whenever an active audio stream is being transmitted, an accurate Audio InfoFrame shall be transmitted at least once per two video fields.

Upon the start of a new audio stream or upon any change in the audio stream that can be indicated by the Audio InfoFrame, a modified, accurate Audio InfoFrame shall be transmitted no later than one video field following the first affected non-silent audio sample. Preferably this would occur just before the first affected audio sample is transmitted.

The Audio InfoFrame transmission may occur at any time that a Data Island packet may be transmitted, including during any horizontal or vertical blanking period.

The following tables show the packetization of the Audio InfoFrame.

Table 8-4 Audio InfoFrame Packet Header

Byte \ Bit #	7	6	5	4	3	2	1	0
HB0	Packet Type = 0x84							
HB1	Version Number = 0x01							
HB2	0	0	0	Length = 10 (0x0A)				

Table 8-5 Audio InfoFrame Packet contents

Packet Byte #	EIA/CEA-861B Byte #	7	6	5	4	3	2	1	0
PB0	n. a.	checksum							
PB1	Data Byte 1	CT3	CT2	CT1	CT0	Rsvd	CC2	CC1	CC0
PB2	Data Byte 2	Reserved			SF2	SF1	SF0	SS1	SS0
PB3	Data Byte 3	Format depends on coding type (i.e. CT0…CT3)							
PB4	Data Byte 4	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
PB5	Data Byte 5	DM_INH	LSV3	LSV2	LSV1	LSV0	Reserved		
PB6	Data Byte 6	Reserved							
PB7	Data Byte 7	Reserved							
PB8	Data Byte 8	Reserved							
PB9	Data Byte 9	Reserved							
PB10	Data Byte 10	Reserved							
PB11-PB27	Data Byte 11-27	Reserved							

- CC0…CC2 Channel Count. See EIA/CEA-861B table 19 for details.
- CT0…CT3 Coding Type. See EIA/CEA-861B table 19 for details. The CT bits shall always be set to a value of 0, 0, 0, 0 (“Refer to Stream Header”).
- SS0…SS1 Sample Size. See EIA/CEA-861B table 20 for details. The SS bits shall always be set to a value of 0, 0 (“Refer to Stream Header”).
- SF0…SF2 Sample Frequency. See EIA/CEA-861B table 20 for details. The SF bits shall always be set to a value of 0, 0, 0 (“Refer to Stream Header”).
- CA0…CA7 Channel/Speaker Allocation. See EIA/CEA-861B Section 6.3.2 for details.
- LSV0…LSV3 Level Shift Value (for downmixing). See EIA/CEA-861B Section 6.3.2 and EIA/CEA-861B table 23 for details.
- DM_INH Downmix Inhibit. See EIA/CEA-861B Section 6.3.2 and table 24 for details. The DM_INH field is to be set only for DVD-Audio applications and corresponds to the value in the DM_INH field of the current audio stream being played from the disk. The DM_INH field value shall be set to zero in all cases other than DVD-Audio applications.

Data Byte 3 must always be set to a value of 0.

8.3 E-EDID Data Structure

All Sinks shall contain an EIA/CEA-861B compliant E-EDID data structure accessible through the DDC.

A Source shall read the EDID 1.3 and first CEA EDID Timing Extension to determine the capabilities supported by the Sink. Additional extensions may be read to discover additional capabilities. The Source is responsible for any format conversions that may be necessary to supply audio and video in an understandable form to the Sink. However, it is permitted for a Source to transmit Basic Audio (see Section 7.3) to a Sink that does not indicate support for Basic Audio.

The overall structure of the E-EDID in the Sink shall conform to the E-EDID structure defined in the VESA E-EDID Standard Release A, Revision 1, but shall also meet the additional requirements specified herein.

The first 128 bytes of the E-EDID shall contain an EDID 1.3 structure. The contents of this structure shall also meet the requirements of EIA/CEA-861B.

8.3.1 EDID Timing Extension

The first E-EDID 'extension' shall contain a CEA EDID Timing Extension version 3, defined in EIA/CEA-861B section 7.5. Additional CEA EDID Timing Extensions may also be present. The E-EDID shall not contain an EDID Timing Extension version 1 or version 2.

EDID Timing Extension version 3 details are described in EIA/CEA-861B Section 7.5.

Further details on the requirements of the data structures in the E-EDID and implementation examples are given in EIA/CEA-861B.

8.3.2 Audio and Video Details

Sink audio characteristics and support are indicated in the E-EDID. This data includes a list of audio encodings supported by the Sink and parameters associated with each of those encodings.

A Sink may indicate support for YC_BC_R pixel encodings. To indicate support, bits 4 and 5 of byte 3 of the EDID Timing Extension shall both be set to one (see Table 29 of EIA/CEA-861B). To indicate no support, bits 4 and 5 shall both be zero.

If a Sink is required to support a particular video format, video format timing, or pixel encoding, then the Sink shall indicate support for that video format, video format timing or pixel encoding in the E-EDID.

8.4 Enhanced DDC

Enhanced DDC described in this section is defined in VESA "ENHANCED DISPLAY DATA CHANNEL STANDARD Version 1 (September 2, 1999)". All Sinks are required to support these enhanced DDC features. If a Sink's E-EDID structure is longer than 256 bytes, it shall support the segment pointer.

8.4.1 Timing

Data is synchronized with the SCL signal and timing shall comply with the Standard Mode of the I^2C specification (100kHz clock).

I^2C Bus is a standard two-wire (clock and data) serial data bus protocol. Refer to the I^2C specification for details.

Note that an HDMI Sink may hold off the DDC transaction by stretching the SCL line during the SCL-low period following the Acknowledge bit as permitted by the I^2C specification. All HDMI Sources shall delay the DDC transaction while the SCL line is being held low.

8.4.2 Data Transfer Protocols

The Source shall use I^2C commands to read information from a Sink's E-EDID with a slave address.

In Enhanced DDC, a segment pointer is used to allow addressing of the E-EDID outside of the normal 256-byte limit of the 0xA0/0xA1 address. The Enhanced DDC protocol sets the segment pointer before the remainder of the DDC command.

8.4.3 Segment pointer

Enhanced DDC allows access of up to 32 Kbytes of data. This is accomplished using a combination of the 0xA0/0xA1 address pair and a segment pointer. For each value of the segment pointer, 256 bytes of data are available at the 0xA0/0xA1 address pair. An unspecified segment pointer references the same data as when the segment pointer is zero.

Each successive value of the segment pointer allows access to the next two blocks of E-EDID (128 bytes each). The value of the segment pointer register cannot be read since it is reset at the completion of each command.

8.4.4 Enhanced DDC Sink

The Sink shall be Enhanced DDC read compliant.

The Sink shall be capable of responding with EDID 1.3 data and up to 255 extension blocks, each 128 bytes long (up to 32K bytes total E-EDID memory) whenever the Hot Plug Detect signal is asserted.

The Sink should be capable of providing E-EDID information over the Enhanced DDC channel whenever the +5V Power signal is provided. This should be available within 20msec after the +5V Power signal is provided.

8.4.5 Enhanced DDC Source

The Source shall use Enhanced DDC protocols.

The Source shall be capable of reading EDID 1.3 data at DDC address 0xA0.

The Source reads Enhanced EDID extensions data at DDC address 0xA0 using segment pointer 0x60.

8.5 Hot Plug Detect Signal

An HDMI Sink shall not assert high voltage level on its Hot Plug Detect pin when the E-EDID is not available for reading. The Hot Plug Detect pin may be asserted only when the +5V Power line from the Source is detected. This will ensure that the Hot Plug Detect pin is not asserted before the Third Make of the connector.

A Source may use a high voltage level Hot Plug Detect signal to initiate the reading of E-EDID data.

An HDMI Sink shall indicate any change to the contents of the E-EDID by driving a low voltage level on the Hot Plug Detect pin for at least 100 msec.

9 Consumer Electronics Control (CEC)

CEC is an optional lightweight protocol within HDMI that provides high-level control functions between the various audiovisual products in a user's environment. CEC is a low-speed bus operating at 400 bits/second and is designed specifically to function with minimal processing and memory overhead.

The mandatory requirements for the CEC line are described in detail in HDMI Specification 1.0, Electrical Specifications section. The optional CEC protocol is described in detail in HDMI Specification 1.0, Supplement 1: Consumer Electronics Control (CEC).

9.1 Device Addressing

All HDMI devices have a Physical Address of the form A.B.C.D. In addition, HDMI devices with CEC capability (i.e. CEC devices) have a Logical Address, which is used to address CEC messages between individual devices. When a CEC device is allocated a valid Physical Address, it attempts to take a Logical Address. Logical Addresses are allocated based on device types (e.g. DVD, STB etc.); therefore, the type of a device may be identified by its Logical Address.

9.2 CEC line usage

A message is conveyed over the CEC line in a single frame; a frame is a self-contained unit consisting of a start bit followed by a number of data bits.

An initiator first has to test that the CEC line is free for use. After that it generates a high to low transition on the CEC line, followed by a series of pulses comprising data bits whose starting point is defined by a high to low transition.

The initiator provides bit timing and bit leading edges. Only one initiator is allowed at any one time. A CEC line arbitration mechanism avoids conflicts when more than one initiator begins transmitting at the same time.

9.3 Messages

The CEC protocol is made up of a number of messages with various parameters.

All transactions on the CEC line are between an initiator and one or more followers. The initiator is responsible for sending the message structure and the data. The follower is the recipient of any data and is responsible for acknowledging the message and reacting as appropriate.

Messages may be directly addressed to a single device or alternatively may be broadcast to all CEC devices within the network.

9.4 Reliable Communications Mechanism

There are three mechanisms in CEC to provide a reliable communications medium for the transfer of frames:

- Frame re-transmissions increase the chance of a successful message transfer.
- Flow control ensures that communication only progresses as fast as the slowest follower.
- Frame validation ensures that any message that does not contain all required parameters is rejected.

9.5 Features

CEC provides a number of recommended features designed to enhance the functionality and interoperability of devices within an HDMI system. A device may implement a sub-set of these features based on its device type and the level of functionality offered. The following list describes the set of features offered:

- **One Touch Play –** A device may be played and become the active source with a single button press.
- **System Standby** – Enables all devices to be switched to standby with a single button press.
- **Preset Transfer** – A device's presets can be auto configured to match those of the TV.
- **One Touch Record –** A recording can be made with a single button press (e.g. via TV).
- **Timer Programming –** Any device can program a timer recording on a recording device.
- **System Information –** A device can auto-configure its language and country settings.
- **Deck Control –** A device can control (e.g. play, fast forward etc.) and interrogate a playback device (a deck).
- **Tuner Control** – Allows a device to manipulate the tuner of another device.
- **Vendor Specific Commands –** Allows vendor-defined commands to be used.
- **OSD Display –** A device can use the on-screen display of the TV to display text strings.
- **Device Menu Control –** Enables a device to control the menu of another device.
- **Routing Control –** Allows the control of CEC Switches for streaming of a new source device.
- **Remote Control Pass Through –** RC commands may be passed through to other devices within the system.
- **Device OSD Name Transfer –** Devices may request the preferred OSD name of other devices within the system.

9.6 Protocol Extensions

In order to allow for extensions to the protocol in future releases of the specification, the current opcodes and parameters can be extended by adding further parameters onto them. For entirely new commands, new opcodes can be allocated. For entirely new device types, new logical addresses can be allocated.

Appendix A Repeater

A.1 Repeater Functions

A Repeater is defined as a device with one or more HDMI inputs and one or more HDMI outputs and a retransmission function.

A Repeater has at least one of following functions:

- Repeat function:
  Single-input, single-output devices. Used primarily for cable extension.
- Switch function:
  Multiple-input, single-output devices. Used primarily to select among multiple Sources.
- Distributor function:
  Single-input, multiple-output devices, where only one output is active. Used primarily to select among multiple displays or Sinks.
- Duplicator function:
  Single-input, multiple-output devices, where more than one output is active. Used for signal distribution.

Combinations of the above, for instance, multiple-input, multiple-output devices, incorporating both input selection and output selection or signal distribution are allowed.

In all cases, each HDMI input shall fulfill all of the requirements of an HDMI Sink when it is connected with an active sink device, and each HDMI output shall fulfill all of the requirements of an HDMI Source when it is connected with an active source.

The E-EDID presented by a Repeater should reflect the capabilities of the downstream Sink.

A.2 E-EDID Read Timing (Informative)

In terms of E-EDID handling, Repeaters will typically fall into one of the following categories.

- Stored E-EDID type: The Repeater stores an E-EDID data structure that typically consists of downstream Sink capabilities.
- Forwarding type: The Repeater does not store an E-EDID data structure. When an E-EDID read request comes from a Source, the Repeater forwards the read request to a Sink. The E-EDID data from the Sink is then forwarded back to the Source.

An HDMI cluster may have several Repeaters between a Source and a Sink. To minimize the impact to the E-EDID reading time, each Repeater in the chain should minimize the added delay.

For example, the delay added by a Forwarding type Repeater should be no more than 4 msec per 16-byte read.

A stored E-EDID type Repeater should be able to send a 256 byte E-EDID within 150 msec when a Source issues sixteen 16-byte read requests. This means that a 16-byte read request would be completed within approximately 10 msec.

Appendix B Type B Connector Usage

B.1 Exception To Audio Format Support Requirement

Sources are not required to carry audio when all of the following conditions are met:

- Source is required by the HDMI Specification or associated agreements to use the Type B connector, and,
- Source has alternate default or user selectable audio outputs, and,
- Source can ensure that the appropriate audio stream is being delivered to the alternate audio outputs.

In order to guarantee rendering of video from Sources that do not fully support HDMI audio, the following condition shall be met:

- Sinks that are capable of supporting an HDMI video format when it is accompanied by audio shall also support that format when it is not accompanied by audio.

It is strongly recommended that a display device, when receiving an HDMI video signal without audio, temporarily indicate to the user that there is no audio accompanying the stream.

B.2 HDMI Dual-Link Architecture

HDMI dual-link architecture is compatible with DVI 1.0 dual-link architecture. Refer to section 3.1.5 of the DVI 1.0 specification.

Appendix C Compatibility With DVI

All HDMI Sources shall be compatible with DVI 1.0 compliant sink devices (i.e. “monitors” or “displays”) through the use of a passive cable converter. Likewise, all HDMI Sinks shall be compatible with DVI 1.0 compliant sources (i.e. “systems” or “hosts”) through the use of a similar cable converter.

When communicating with a DVI device, an HDMI device shall operate according to the DVI 1.0 specification, with the following exception – these devices are not required to comply with DVI 1.0 rules regarding:

- Monitor scaling requirements [refer to Section 2.2.8.2 of the DVI specification – superceded by HDMI specifications]
- Physical Interconnect specifications [refer to Chapter 5 of the DVI specification – superceded by HDMI specifications]
- System Low Pixel Format Support Requirements [refer to Section 2.2.4 of the DVI specification – superceded by HDMI specifications]

Furthermore, for HDMI devices which do not have a “BIOS” or “operating system”, there are the following additional exceptions:

- “BIOS” requirements [refer to Section 2.2.4 of the DVI specification]
- “Operating system” requirements [refer to Section 2.2.2 and Section 2.2.9 of the DVI specification]
- “System level event” requirements [refer to Section 2.2.9.1 of the DVI specification]
- Power management requirements [refer to Section 2.4 of the DVI specification]

