L64014 PC Card Bridge

Technical Manual

Draft 7/28/98

Preliminary

LSI LOGIC®

This document is preliminary. As such, it contains data derived from functional simulations and performance estimates. LSI Logic has not verified either the functional descriptions, or the electrical and mechanical specifications using production parts.

DB14-000042-00, First Edition (July 1998)
This document describes Revision A of LSI Logic Corporation's L64014 PC Card Bridge chip and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

To receive product literature, call us at 1.800.574.4286 (U.S. and Canada); +32.11.300.531 (Europe); 408.433.7700 (outside U.S., Canada, and Europe) and ask for Department JDS; or visit us at http://www.lsilogic.com.

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Preface

This book is the primary reference and technical manual for the L64014 PC Card Bridge. It contains a complete functional description of the L64014 as well as complete physical and electrical specifications.

Audience

This document assumes that you have some familiarity with the specifications of DVD and related digital A/V devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the L64014 chip for possible use in a system
- Engineers who are designing the L64014 chip into a system

Organization

This document has the following chapters and appendixes:

- Chapter 1, Introduction, presents an overview of the L64014.
- Chapter 2, Functional Description, describes the functional blocks within the L64014.
- Chapter 3, Registers, describes the direct and indexed I/O registers, as well as the PC Card configuration and indirect access registers.
- Chapter 4, Signals, defines each of the L64014's I/O signals.
- Chapter 5, Specifications, presents the L64014's electrical characteristics, requirements, and timing, as well as its pinout and package specifications.

Related Publications

PC Card Standard

L64020 DVD Audio/Video Decoder Technical Manual, May 1998, Document No. DB14-000028-00

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” before the number—for example, 0x32CF. Binary numbers are indicated by the prefix “0b” before the number—for example, 0b0011.0010.1100.1111.

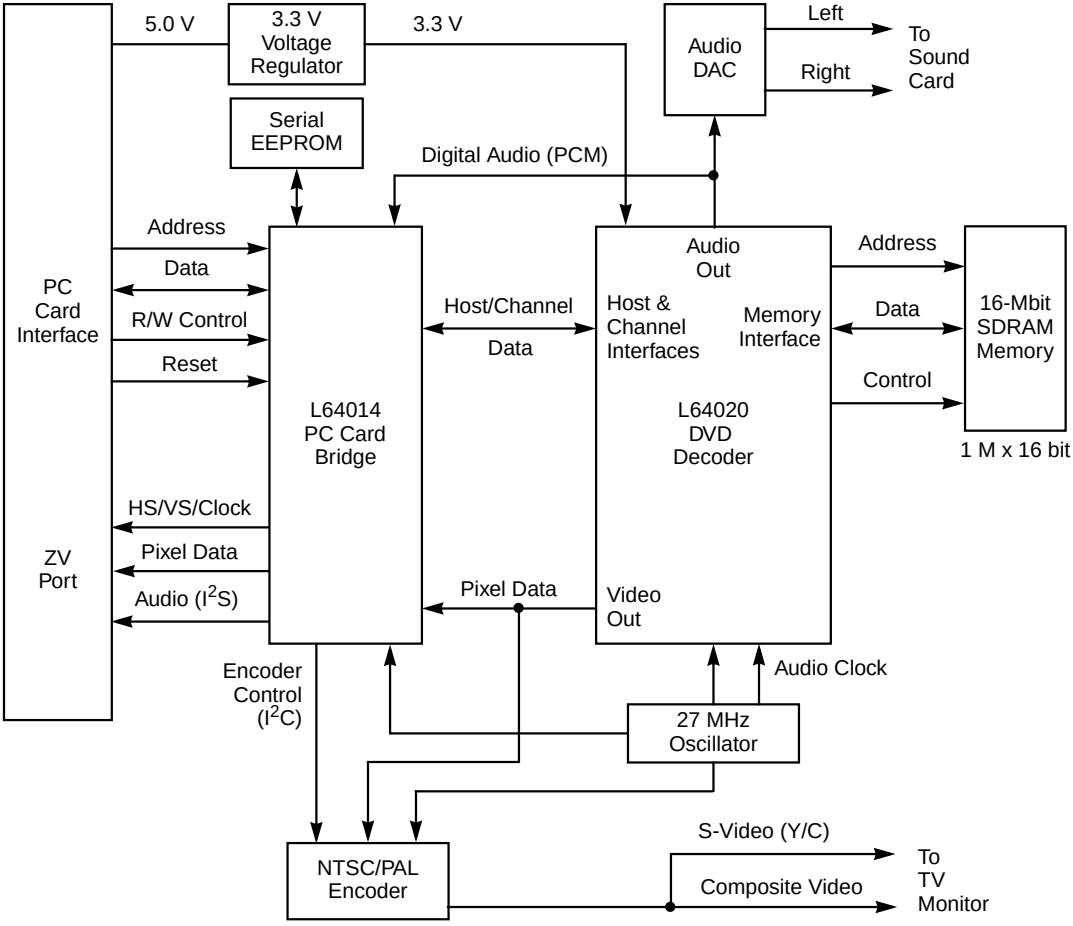
Chapter 1
Introduction

This chapter introduces the L64014 PC Card Bridge and includes these sections:

1.1 Overview

The L64014 PC Card Bridge chip provides a PC Card solution for interfacing a DVD decoder, such as LSI Logic’s L64020, with a low-power notebook computer that is equipped with a Zoomed Video (ZV) port. Figure 1.1 shows a block diagram of the L64014 in a typical system application, which incorporates LSI Logic’s L64020 DVD A/V Decoder. The decoded video output can be viewed on the PC notebook’s monitor, or on an external TV screen by means of an NTSC/PAL video encoder. The L64014 supplies decompressed audio through the ZV port as I^2S formatted stereo. The L64014’s host interface provides host access to its internal control registers, as well as those of the DVD decoder and the NTSC/PAL encoder (I^2C). Its DVD decoder interface includes a look-up table for gamma correction on the YUV pixel data for ZV output. The DVD decoder interface also includes a content scramble system (CSS) module for disc and title key decoding.

Figure 1.1 L64014 Typical Application



1.2 Features

- PC Card interface
- L64020 DVD A/V Decoder interface
- Software-configurable ZV port interface
- Serial EEPROM interface
- Frequency-selectable audio clock control
- ZV signal gamma correction using software look-up table
- External ZV port control
- CSS decoding for DVD playback
- NTSC/PAL encoder interface (I^2C bus control)
- NTSC/PAL video sync from a single 27-MHz clock
- Accepts AES digital audio format and issues I^2S data (ZV port)
- Six GPIO pins
- 144-pin TQFP package

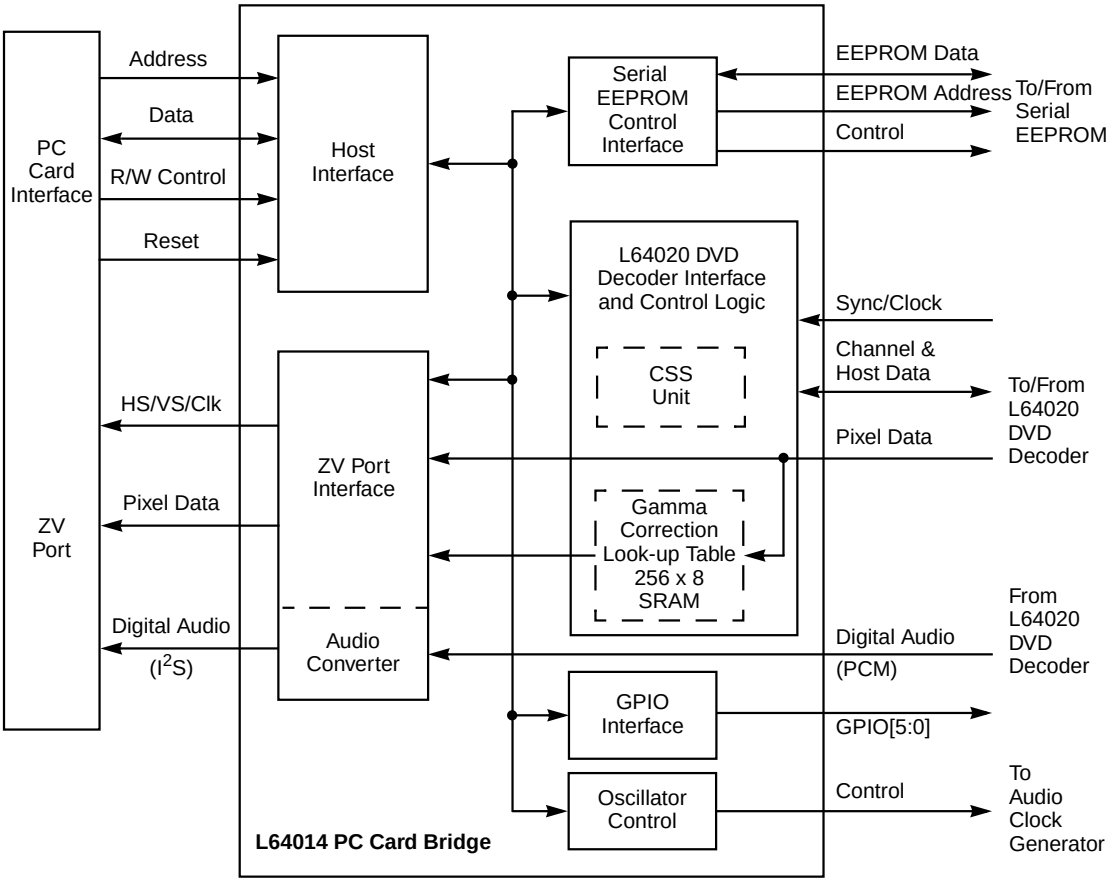
Chapter 2
Functional Description

This chapter provides a functional description of the L64014 and includes these sections:

2.1 Overview

Figure 2.1 shows a functional block diagram of the L64014. The sections that follow this figure describe the functionality of each block.

Figure 2.1 L64014 Functional Block Diagram



2.2 Host Interface

This interface provides the host with access to the L64014 registers for controlling system-level capabilities such as interrupts, reset, wait, and port enabling. Through this interface, the host can read from and write to the direct and indexed registers in the L64014. The host can also access registers in the DVD decoder chip, as well as read data from the serial EEPROM (see Section 2.4, “Serial EEPROM Interface.”)

The L64014 Host Interface supports host access to three PC Card memory address spaces:

- Attribute Memory Space
- Common Memory Space
- I/O Address Space

The host can access the 16-bit PC Card Attribute Memory Space with memory read and write operations that occur while the PCREG_N signal is LOW. This address space is defined only for bytes located at even byte addresses. It is the primary location for the Card Information Structure (CIS) and for the PC Card configuration registers, in particular, the Configuration Option Register (Offset 0, see Section 3.4, “Configuration Option Register.”)

The Common Memory Space is accessed by the host with memory read and write operations that occur while the PCREG_N signal is HIGH. This address space is defined for bytes located at both even and odd byte addresses. The Indirect Access Registers (Offset 2-9) are located in this memory space (Section 3.5, “Indirect Access Registers.”)

The host accesses the I/O Address Space by asserting either the I/O Read signal (PCIORD_N), or the I/O Write signal (PCIOWR_N), while the PCREG_N signal and at least one card enable signal (PCCE1_N and/or PCCE2_N) are LOW. The I/O Address Space contains the six L64014 direct I/O registers, which are used to control the bridge chip. It also includes the 18 indexed I/O registers (for details, see Section 3.3, “Indexed I/O Registers.”)

The L64014 uses the PC Card Indirect Access Registers to support read operations from the EEPROM. These registers are required since the

L64014 only uses four address lines to access the EEPROM's 512 x 8 bits of memory.

Through the Host Interface, the L64014 responds to the following 8-bit commands:

- I/O read and write commands
- Attribute memory read and write commands
- Common memory read and write commands

Table 2.1 shows the active signals that are used for read/write access to/from the L64014.

Table 2.1 L64014 Read/Write Access Signals

Function	PCREG_N (DACK)	PCCEx_N	PCOE_N	PCWE_N	PCIORD_N	PCIOWR_N
I/O Read	L	L	H	H	L	H
I/O Write	L	L	H	H	H	L
Attribute Memory Read	L	L	L	H	H	H
Attribute Memory Write	L	L	H	L	H	H
Common Memory Read	H	L	L	H	H	H
Common Memory Write	H	L	H	L	H	H

2.3 DVD Decoder Interface and Control

The DVD Decoder Interface and Control logic provides access to the DVD Decoder's indexed registers and data ports. The interface and control functions handle register addressing, port enabling, reset, wait, and interrupt control. The control logic generates the required horizontal and vertical synchronization signals (HS and VS_N) for the DVD Decoder. The interrupt control logic receives interrupt requests from the DVD Decoder and relays them to the host.

The HS and VS_N signals are active HIGH outputs that are derived from the DVDCLK input signal. The HS pulse width is 63 clock cycles,

whereas the VS_N pulse width is ??? clock cycles. The video mode (NTSC/PAL/PAL24) determines the horizontal and vertical sync periods as shown in Table 2.2. These video modes can be selected by writing to bits [1:0] in the Video Control 1 Register (0x0A).

Table 2.2 Horizontal and Vertical Sync Periods

Video Mode	Horizontal Sync Period (Clock Cycles)	Vertical Sync Period (Clock Cycles)
NTSC	1716	525
PAL	1728	625
PAL24	1925	585

There are two byte-wide data paths between the DVD Decoder and the L64014. Both paths share the same L64014 data port: AD[7:0].

One data path is for Host access of the registers inside the DVD decoder; control for this path is provided by the AS_N, DS_N, and RD/WR_N signals. The host indirectly accesses DVD decoder registers through the L64014 by writing their addresses to the L64014's LSI Low and High Index Address registers (0x8 and 0xC). When data is read from or written to the LSI Data Register (0xA), the L64014 generates a host/DVD decoder read/write cycle.

The other data path serves as the DVD decoder input path for the encoded MPEG bitstream, which is also called the Channel Data path. This path uses the VVALID_N and AVALID_N signals to indicate that valid data is present on the AD[7:0] bus. Channel data is written to the LSI Decoder Channel Data Register (0x4, W). The audio and video channels are selected by writing to bit 6 in the LSI Control Register (0x06).

2.3.1 GAMMA Correction Look-up Table

The L64014 DVD Decoder Interface includes a 256 x 8-bit SRAM that contains gamma correction information. The information is arranged in a look-up table. When the gamma correction look-up function is enabled, the incoming 8-bit pixel data from the DVD Decoder is used as the

address for accessing the correct SRAM location. Each SRAM location contains gamma corrected video luminance information. The L64014 accesses the information in the look-up table, and sends this information to the ZV port (through ZV_YV[7:0]) in place of the luminance video data that originated from the L64020.

The Video Look-up Table Data Port Register (0x0B, W) provides a path for writing gamma correction data into SRAM. This data port is always enabled. By setting bit 2 in the Video Control 1 Register (0x0A), the host can enable read operations from the gamma correction look-up table.

2.3.2 Content Scramble System (CSS)

The L64014 DVD Decoder Interface features a CSS component for descrambling DVD disc and title keys. These keys provide access to protected data on the DVD disc. The CSS Key Register (0x14) holds the 8-bit disc and title keys during the descrambling process. The host can control CSS functions by writing to the CSS Command Register (0x12). It can also monitor CSS operations by reading the CSS Status Register (0x13).

2.4 Serial EEPROM Interface

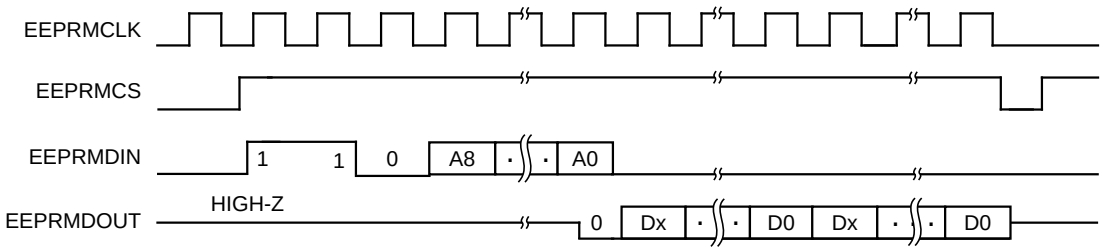
The L64014 EEPROM Interface provides a serial interface to the external EEPROM. Because this is a serial interface, the memory pinout requirements are greatly reduces.

The EEPROM contains card information structure (CIS) data. The host can read or write CIS data through the L64014 in serial, as well as in parallel, one byte at a time. Typically, CIS transfers are parallel operations. Setting the bits in the EEPROM Control Register (0x0C) enables the host to write data to the EEPROM. Software is required for the host to directly control the EEPROM signals.

Figure 2.2 shows the timing for read operations. The host uses the Indirect Access Address Register to address the EEPROM (see Section 3.5, “Indirect Access Registers”.) Since the L64014 Serial EEPROM Interface always sends 9 address bits, the dimensions of the EEPROM memory space must be 512 x 8 bits. Only the least significant 9 bits of the Indirect

Access Address Register (Common Memory offset 4-7) are used for addressing the EEPROM.

Figure 2.2 EEPROM Read Timing



The host initiates parallel read transfers by executing the PC Card Read Attribute Memory command, or the Read Common Memory command. When one of these read commands is issued, the L64014 reads the data serially from the EEPROM, assembles it, and then sends it to the host one byte at a time. While accessing attribute memory, the host only reads the even bytes of the EEPROM address space. While accessing common memory, the host reads both the even and odd bytes of the EEPROM address space.

Note: The EEPROM must have a minimum clock speed of 3 MHz.

2.5 Zoomed Video (ZV) Port Interface

The ZV port interface supplies the host system with decoded 8-bit or 16-bit YUV pixel data and I^2S formatted digital serial audio data. The L64014 zoomed video logic also outputs a horizontal sync (ZV_HREF_N) signal, a vertical sync (ZV_VREF) signal, and a pixel clock (ZV_PIXCLK) signal. These signals are derived from the 27-MHz system clock that is used by the L64020 DVD A/V Decoder.

The host can select the pixel data output width by writing to bit 4 in the Video Control 0 Register (0x09). The L64014 sends 8-bit pixel data when bit 4 is zero; setting this bit configures the L64014 to send 16-bit pixel data. In 8-bit mode, YUV data is sent on the ZV_Y[7:0] lines. In 16-bit mode, luminance (Y) data is sent on the ZV_Y[7:0] lines and chrominance (UV) data is sent on the ZV_UV[7:0] lines.

For 8-bit video output, ZV_PIXCLK runs at 27 MHz. For 16-bit video output, the 27-MHz clock can be divided to generate a 13.5-MHz ZV_PIXCLK signal by setting bit 2 in the Video Control 0 Register (0x09).

The host can also enable optional gamma correction on pixel data for ZV output by setting bit 2 in the Video Control 1 Register (0x0A).

The L64020 DVD Decoder supplies 32-bit sign-extended PCM audio data in right-justified frames. By setting bit 4 in the Oscillator and Audio Control Register (0x08), the L64014's ZV interface logic converts the PCM data to digital stereo I^2S. The SDATA signal carries the I^2S serial audio data to the ZV port. A DAC within the PC converts the I^2S data to analog for playback on speakers.

2.6 GPIO Interface

The L64014 GPIO Interface comprises six general purpose I/O lines (GPIO[5:0]). These lines can be used to supply I^2C control to an external NTSC/PAL video encoder. By setting bits in the GPIO Control (0x10) and GPIO Pins (0x11) indexed registers, the host can send data across the GPIO[5:0] lines.

2.7 Oscillator Control Interface

The L64014 Oscillator Control Interface logic provides host control of an external oscillator. The L64014 receives a 27-MHz system clock from this oscillator. By writing to the Oscillator and Audio Control Register (0x08), bits [3:0], the host can select the audio clock frequency, as well as place the oscillator in Sleep mode.

Chapter 3
Registers

This chapter describes the L64014 internal registers and includes the following sections:

3.1 Overview

The L64014 registers are located in three distinct address spaces:

- Attribute Memory Space
- Common Memory Space
- I/O Address Space

The Attribute Memory Space contains the Configuration Option Register (offset 0). The Indirect Access Registers (offset 2-9) are located in the Common Memory Space. The I/O Address Space contains the L64014-specific direct and indexed I/O registers. The host can address these registers using read/write commands. Indirect addressing reduces pin requirements; the L64014 only uses four address lines to access these memory spaces.

Note: The L64014 must be configured by the system before the I/O Address Space can be accessed.

The L64014 features six direct and 18 indexed I/O registers. The HA[3:0] pins supply host access to the direct I/O registers. Two of the direct I/O

registers provide read/write access to the L64014's indexed I/O registers. The other direct I/O registers provide read/write access to the registers in the L64020 DVD A/V Decoder. They also supply status information on the DVD decoder interface.

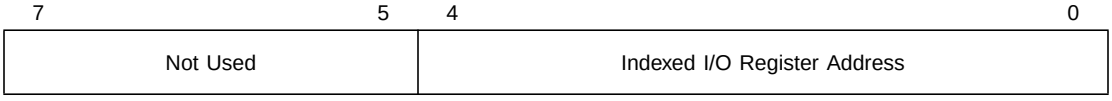
3.2 Direct I/O Registers

Table 3.1 lists the six direct I/O registers and their addresses. Each register is addressed using a 4-bit address. (Note that the L64014 does not use PC Card address bits 4 and 5 (HA4, HA5).)

Table 3.1 Direct I/O Register Map

Offset Address	R/W	Bit Width	Register Name
0x0	R/W	5	Control Index Register
0x2	R/W	8	Control Data Register
0x4	R	4	LSI Decoder Status Register
	W	8	Channel Data Register
0x8	R/W	8	LSI Low Index Address Register
0xA	R/W	8	LSI Data Register
0xC	R/W	1	LSI High Index Address Register

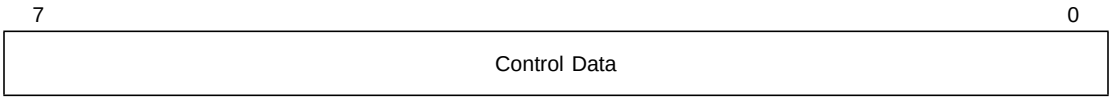
3.2.1 Control Index Register (0x0)



Not Used **7:5**

Indexed I/O Register Address **R/W 4:0**
This register contains the address for a specified indexed I/O register. (See Table 3.2 for a list the Indexed I/O Register addresses.) The Control Data Register (0x2) writes and reads data to and from the I/O register whose address is referenced in this register.

3.2.2 Control Data Register (0x2)



Control Data **R/W 7:0**
This register reads data from and writes data to the indexed I/O register whose address is specified in the Control Index Register (0x0).

3.2.3 LSI Decoder Status Register (0x4)

	7 … 4	3	2	1	0
Read	Not Used	RE	Wait	ARQ	VRQ
Write	Channel Data				

The read portion of this register contains DVD decoder status information. The write portion contains channel data.

Not Used **R 7:4**

RE **Ready Error** **R 3**
The L64014 sets this bit when the Wait state times out (WAIT_N is LOW for 128 DVDCLK cycles). The Ready Error bit is cleared by setting bit 5 in the LSI Control Register (0x06).

Wait **R 2**
This bit is cleared when the WAIT_N input signal (pin 5) from the DVD decoder is asserted (LOW).

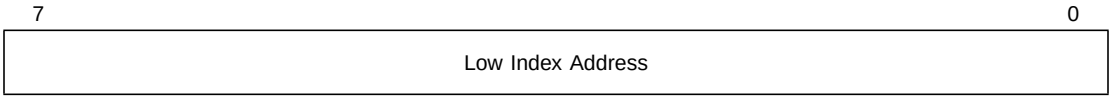
ARQ **Audio Request** **R 1**
This audio request bit is cleared when the AREQ_N input signal (pin 21) from the DVD decoder is asserted (LOW).

VRQ **Video Request** **R 0**
This video request bit is cleared when the VREQ_N input signal (pin 23) from the DVD decoder is asserted (LOW).

Channel Data **W 7:0**
When 8-bit channel data is written to this register, the L64014 outputs the data to the DVD decoder through the

AD[7:0] bus. The channel control signals (AREQ_N, VREQ_N, AVALID_N, and VVALID_N) strobe the bit-stream data into the L64020. Setting or clearing bit 6 in the LSI Control Register (0x06) selects the video channel or the audio channel, respectively.

3.2.4 LSI Low Index Address Register (0x8)



Low Index Address **R/W 7:0**

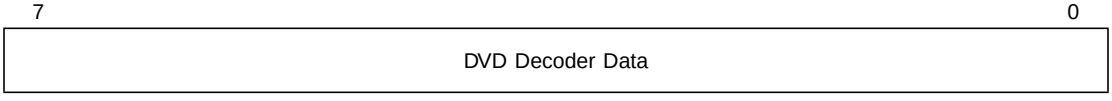
This dual-purpose register holds either of the two following types of address information:

- the lower eight bits of the of the 9-bit LSI indexed I/O register address
- the address of a SRAM location that contains gamma correction data for YUV output through the ZV port

In the first case, when host data is written to or read from the LSI Data Register (0xA), it is cycled to/from the decoder using the address that is specified by concatenating the contents of this register with that of the LSI High Index Address Register (0xC).

In the second case, the L64014 stores the gamma correction information in a RAM look-up table. When data is written to the Video Look-up Table Data Port Register (0x0B), it is cycled to the look-up table SRAM using the address specified by this register.

3.2.5 LSI Data Register (0xA)

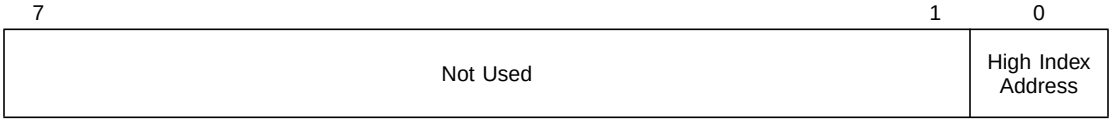


DVD Decoder Data **R/W 7:0**

The host uses this register to read/write data from/to the DVD decoder register whose address is obtained by concatenating the contents of the LSI Low and High Index Address Registers (0x8 and 0xC, respectively). When

this register is written or read, its contents is sent across the AD[7:0] lines. These host/decoder data transfers are controlled using the AS_N, CS_N, DS_N, and RD/WR_N signals.

3.2.6 LSI High Index Address Register (0xC)



High Index Address **R/W 0**

This register holds the highest bit of the 9-bit LSI indexed register address. When host data is written to or read from the LSI Data Register (0xA), it is cycled to/from the decoder using the address that is specified by concatenating the contents of this register with that of the LSI Low Index Address Register (0x8).

3.3 Indexed I/O Registers

The L64014 includes 18 indexed I/O registers. Table 3.2 provides a map of the indexed registers.

Table 3.2 Indexed I/O Register Map

Offset Address	R/W	Bit Width	Register Name
0x00	R	8	ID Register
0x01	R	8	Mode Register
0x02	R/W	8	IRQ Control Register
0x03	R	8	IRQ Status Register
0x06	R/W	8	LSI Control Register
0x08	R/W	6	Oscillator and Audio Control Register
0x09	R/W	5	Video Control 0 Register
0x0A	R/W	8	Video Control 1 Register
0x0B	W	8	Video Look-up Table Data Port Register
0x0C	R/W	4	EEPROM Control Register
0x0D	R/W	8	Video Horizontal Delay Register
0x0E	R/W	8	Video Horizontal Active Register
0x0F	R/W	7	Video Horizontal High Bits Register
0x10	R/W	6	GPIO Control Register
0x11	R/W	6	GPIO Pins Register
0x12	R/W	5	CSS Command Register
0x13	R/W	2	CSS Status Register
0x14	R/W	8	CSS Key Register

3.3.1 ID Register (0x00)

7	6	5	4	3	2	1	0
1	1	0	1	1	1	0	1

ID Register **R 7:0**
This read-only register is hardcoded with the L64014 device ID, which is 0xDD.

3.3.2 Mode Register (0x01)

7 — 3	2 — 0
Chip Version	Operating Mode

Chip Version **R 7:3**
This read-only field contains the chip version number.

Operating Mode **R 2:0**
This read-only field specifies the L64014 operating mode. These bits are set to 0b010 for normal PC Card operation.

Bits 2:0	Function
010	Normal PC Card operation
011	Reserved for 3-state output test
111	Reserved for scan flip-flop test

3.3.3 IRQ Control Register (0x02)

7	6	5	4	3	2	1 — 0
IVVE	Reserved	IDE	ILT	IM	IE	Reserved

The contents of this register controls interrupt requests (IRQs). The PCIRQ_N output signal is generated from the VS_N and IRQ_N input signals, which are passed directly through the DVD decoder interface.

IVVE **IRQ Video Vertical Sync Enable** **R/W 7**
Setting this bit allows the VS_N signal to generate the PC_IRQ_N interrupt output. Clearing this bit disables this feature and clears bit 6 in the IRQ Status Register (0x03).

Reserved (must be set to 0) **6**

IDE **IRQ DVD Enable** **R/W 5**
Setting this bit allows the IRQ_N signal to generate the PC_IRQ_N interrupt output. Clearing this bit disables this feature and clears bit 4 in the IRQ Status Register (0x03).

ILT **IRQ Low True** **R/W 4**
Setting this bit changes the interrupt polarity of the PCIRQ_N output signal to active HIGH. Clearing this bit maintains the interrupt polarity of the PCIRQ_N output signal as active LOW (normal PC Card operation).

IM **IRQ Mask** **R/W 3**
Setting this bit masks the interrupts. Clearing this bit enables the interrupts. Bit 2 of this register must be set for this bit to mask the interrupts.

IE **IRQ Enable** **R/W 2**
Setting this bit enables the interrupts. Clearing this bit disables the interrupts.

Reserved (must be set to 0) **1:0**

3.3.4 IRQ Status Register (0x03)

7	6	5	4	3	2	1	0
Not Used	VID VSIRQ	Reserved	DVDIRQ	Not Used			

This register contains the interrupt status information. It is a latched version of each IRQ.

Not Used **7**

VIDVSIRQ **Video Interrupt** **R 6**
When set, this bit indicates that an interrupt is initiated on the falling edge of the DVD decoder VS_N signal. This bit is cleared when bit 7 in the IRQ Control Register (0x02) is cleared.

Reserved **5**

DVDIRQ **DVD Decoder Interrupt** **R 4**
When set, this bit indicates that an interrupt is initiated on the falling edge of the DVD decoder IRQ_N signal. This bit is cleared when bit 5 in the IRQ Control Register (0x02) is cleared.

Not Used **3:0**

3.3.5 LSI Control Register (0x06)

7	6	5	4	1	0
Not Used	DSVC	RR	Not Used		DR

This register controls DVD decoder channel selection, decoder reset, and ready error reset.

Not Used **7**

DSVC **Decoder Select Video Channel** **R/W 6**
This bit selects which A/V channel data control signals (AVALID_N or VVALID_N) are used when writing to the Channel Data Register (0x4, W).

Setting this bit selects the video channel (VVALID_N is used). Clearing this bit selects the audio channel (AVALID_N is used).

RR **Ready Reset** **R/W 5**
Setting this bit resets Ready Error (bit 3) in the LSI Decoder Status Register (0x4, R).

Not Used **4:1**

DR **LSI Decoder Reset** **R/W 0**
This bit controls the DVD decoder reset signal, RST_N (pin 8).

Clearing this bit drives RST_N LOW, which resets the DVD decoder. Setting this bit drives RST_N HIGH.

3.3.6 Oscillator and Audio Control Register (0x08)

7	6	5	4	3	2	1	0
Not Used		AF1	AF0	SLEEP	AFS2	AFS1	AFS0

This register provides oscillator frequency and audio control functions.

Not Used **7:6**

AF1 **Audio Form 1** **R/W 5**
Reserved

AF0 **Audio Form 0** **R/W 4**
Setting this bit controls the L64014 to convert DVD decoder digital PCM audio data (ASDATA) to I^2S format before sending it to the SDATA output. Clearing this bit causes the DVD decoder to send the ASDATA signal directly to the SDATA output.

SLEEP **Oscillator Sleep Mode Control** **R/W 3**
This bit directly drives the Oscillator Sleep output signal (OSC_SLP, pin 103). It can be used to disable the external DVDCLK and audio clocks to reduce power consumption.

Setting this bit asserts OSC_SLP (HIGH), thereby enabling Oscillator Sleep mode. Clearing this bit drives

OSC_SLP LOW, thereby returning the oscillator to normal operation.

AFS2:0 **Audio Frequency Select 2:0** **R/W 2:0**

The frequency select bits, AFS2:0, directly control pins 120 (OSC_AS2), 117 (OSC_AS1), and 119 (OSC_AS0), respectively. These pins connect to the external audio clock generator.

When using a Microclock 2744 or 2745-21 oscillator, these three bits select the audio master clock frequency as shown below:

AFS2	AFS1	AFS0	Audio Clock Frequency (in MHz)
0	0	0	12.288
0	0	1	11.2896
0	1	0	8.192
0	1	1	24.576
1	0	0	8.192
1	0	1	16.9344
1	1	0	18.432
1	1	1	11.2896

3.3.7 Video Control 0 Register (0x09)

7 5	4	3	2	1	0
Not Used	ZV16Bit	ZVCLK INV	ZVCLK13	SWAP	VSBT

Not Used **7:5**

ZV16Bit **ZV 16 Bit** **R/W 4**

When this bit is set, the ZV port enters the 16-bit mode. In this mode, Y pixel data is made available on ZV_Y7:0 (pins 105, 104, 102:97) and UV pixel data on ZV_UV7:0 (pins 94:92, 90:88, 86, 84)

When this bit is cleared, the ZV port enters the 8-bit mode. In this mode, YUV pixel data is made available on ZV_Y7:0 (pins 105, 104, 102:97)

ZVCLKINV **ZV Clock Invert** **R/W 3**

Setting this bit inverts the ZV_PIXCLK output signal. When this bit is cleared, the ZV_PIXLCK signal is output without inversion.

ZVCLK13 **ZV Clock 13 Select** **R/W 2**

When this bit is set, a 13.5-MHz clock is output on ZV_PIXCLK (pin 80) for 16-bit mode operation. When this bit is cleared, a 27-MHz clock is output on ZV_PIXCLK (pin 80) for 8-bit mode operation.

FLDSWAP **Field Swap** **R/W 1**

Setting this bit starts the odd field on line 1 (bottom display field becomes odd field). Clearing this bit starts the odd field on line zero (top display field becomes odd field).

VSBT **VS Type B** **R/W 0**

When this bit is set, bottom/top field toggling for each field is made available on VS_N (pin 142). Clearing this bit allows video sync to be generated from the 27-MHz clock for output on VS_N (pin 142).

3.3.8 Video Control 1 Register (0x0A)

7	6	5	4	3	2	1	0
ZVE	ZVO	ZHSN	ZHRN	ZVRFN	ELUT	VMS	

ZVE **ZV Enable** **R/W 7**

Setting this bit enables zoomed video output on the host ZV port. Clearing this bit isolates all ZV signal pins

ZVO **ZV Override** **R/W 6**

This bit, in combination with bit 7 of this register, controls access to the ZV port. The ZV_ENABLE and ZV_ON signals together can 3-state the ZV output pins and also indicate, through ZV_ON, that the ZV port is isolated from the L64014.

When this bit is set, the L64014 ZV interface overrides the state of ZV_ENABLE (pin 27) and enables the ZV

output. Clearing this bit allows ZV_ENABLE (pin 27) to control all ZV signal pins.

Bit 7	Bit 6	ZV_ENABLE Input Signal	ZV_ON Output Signal	ZV Signal Pins
0	0	0	0	High Z
0	0	1	0	High Z
0	1	0	0	High Z
0	1	1	0	High Z
1	0	0	0	High Z
1	0	1	1	Active
1	1	0	1	Active
1	1	1	1	Active

ZHSN **ZV HS Negative** **R/W 5**

Setting this bit inverts the polarity of the ZV_HS signal (pin 75) with respect to the DVD decoder HS signal. When this bit is cleared, the ZV_HS signal has the same polarity as the DVD decoder HS signal.

ZHRN **ZV HRF Negative** **R/W 4**

Setting this bit inverts the polarity of ZV_HREF_N (pin 83) with respect to the HACTIVE signal. When this bit is cleared, the ZV_HREF_N signal has the same polarity as HACTIVE (positive) signal.

HACTIVE is an internal signal that is defined and controlled by the three Horizontal Control registers (0x0D, 0x0E, 0x0F).

ZVRFN **ZV VRF Negative** **R/W 3**

Setting this bit inverts the polarity of the ZV_VREF signal (pin 81) with respect to the DVD decoder VS_N signal. When this bit is cleared, the ZV_VREF signal has the same polarity as VS_N signal.

ELUT **Enable LUT** **R/W 2**

This bit enables read operations from the gamma correction look-up table.

When this bit is set, the L64014 uses the Y pixel data from the DVD decoder as an address to the gamma correction look-up table (in SRAM). Gamma corrected pixel

data is output through ZV_Y[7:0] on pins 105,104, and 102:97.

When this bit is cleared, Y pixel data from the DVD decoder is output directly to ZV_Y[7:0] on pins 105,104, and 102:97.

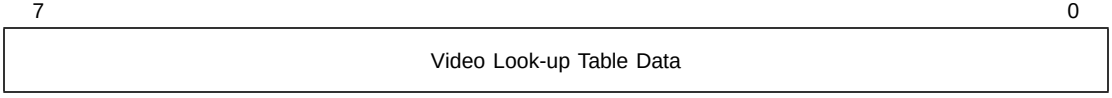
VMS **Video Mode Select** **R/W 1:0**

These bits select the NTSC/PAL video mode as shown in the following table:

Bit 1	Bit 0	Description
0	0	No sync generation[1]
0	1	NTSC sync generation
1	0	PAL sync generation
1	1	PAL24 sync generation

1. In this mode, horizontal and vertical sync signals are 3-stated.

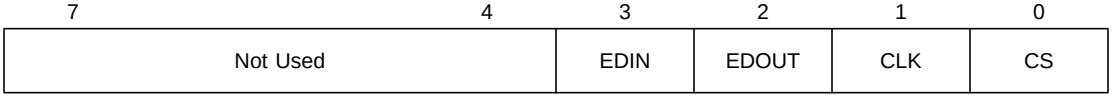
3.3.9 Video Look-Up Table Data Port Register (0x0B)



Video Look-up Table Data **W 7:0**

When data is written to this register, the L64014 passes it through directly to the Gamma Correction Look-Up Table located in SRAM. The address to which this data is written is specified in the LSI Low and High Index Address registers (0x8 and 0xC). The look-up table data port is always enabled.

3.3.10 EEPROM Control Register (0x0C)



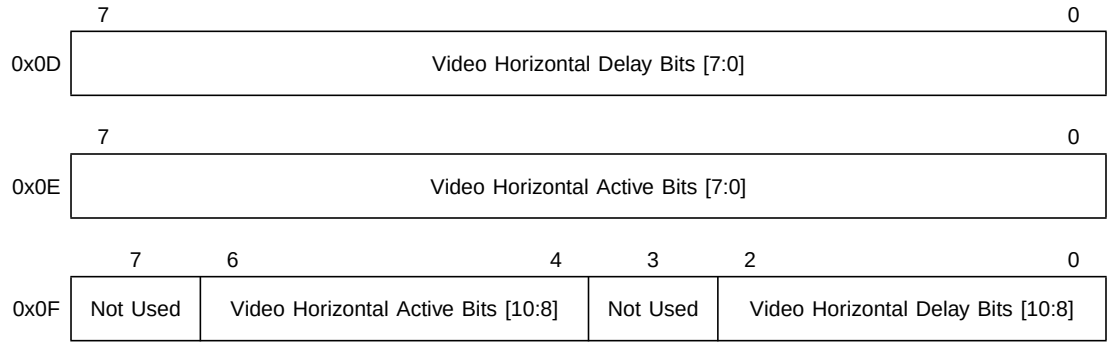
This register allows the software to completely control EEPROM read and write operations. The data can be written to or read from the EEPROM device during normal serial operations. Serial operations that

read the EEPROM directly use the bits in this register to control the EEPROM signals.

The EEPROM Control Register is not used during byte parallel operations. In this mode, all bits in this register must be cleared.

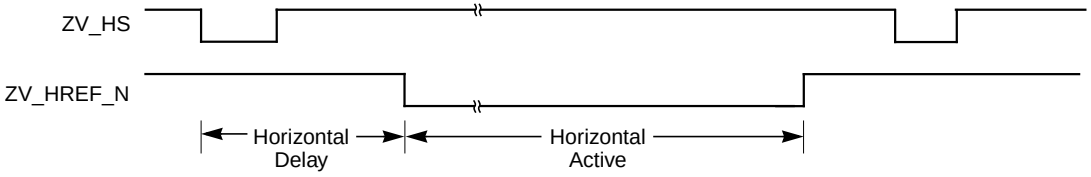
	Not Used	**7:4**
EDIN	**EEPROM Data Input**	**R 3**
	When pin 78 (EEPRMDIN) is driven HIGH, this bit is set, thereby enabling data input to the L64014 from the EEPROM. When pin 78 goes LOW, this bit is cleared.	
EDOUT	**EEPROM Data Output**	**R/W 2**
	Setting this bit drives pin 77 (EEPRMDOUT) HIGH, thereby enabling data output to the EEPROM. Bit 0 in this register must be set before this bit takes effect. Clearing this bit drives pin 77 LOW.	
CLK	**EEPROM Serial Clock**	**R/W 1**
	Setting this bit drives pin 64 (EEPRMCLK) HIGH, thereby enabling the L64014 serial clock output to the EEPROM. Bit 0 in this register must be set before this bit takes effect. Clearing this bit drives pin 64 LOW.	
CS	**EEPROM Chip Select**	**R/W 0**
	Setting this bit drives pin 60 (EEPRMCS) HIGH, thereby enabling the EEPROM chip select signal. This bit must be set before bits 2:1 in this register become effective. Clearing this bit drives pin 60 LOW.	

3.3.11 ZV Horizontal Reference Control Registers (0x0D-0x0F)



Registers 0x0D, 0x0E, and 0x0F control the waveform of the ZV_HREF_N signal, which provides the active period during which pixels are displayed on the video monitor. The period of the ZV_HREF_N signal is the same as that of the ZV_HS signal. Figure 3.1 shows the relationship between the waveforms of these two signals.

Figure 3.1 ZVHREF Output Timing



Horizontal Delay is the duration of time, in DVDCLK cycles, between the active (falling) edge of the ZV_HS signal and the active (falling) edge of the ZV_HREF_N signal. This parameter can be specified by writing to the Video Horizontal Delay Bits [10:0] in registers 0x0D (bits [7:0]) and 0x0F (bits [2:0]).

Horizontal Active is the time, in DVDCLK cycles, during which the ZV_HREF_N signal is active (LOW). This parameter can be specified by writing to the Video Horizontal Active Bits [10:0] in registers 0x0E (bits [7:0]) and 0x0F (bits [6:4]).

Video Horizontal Delay Bits [7:0] (0x0D) R/W 7:0
This register contains the lower eight bits of the 11-bit Horizontal Delay parameter. The contents of this register

is concatenated with the contents of Register 0x0F, bits [2:0], to form the full value of this parameter.

Video Horizontal Active Bits [7:0] (0x0E) R/W 7:0
This register contains the lower eight bits of the 11-bit Horizontal Active parameter. The contents of this register is concatenated with the contents of Register 0x0F, bits [6:4], to form the full value of this parameter.

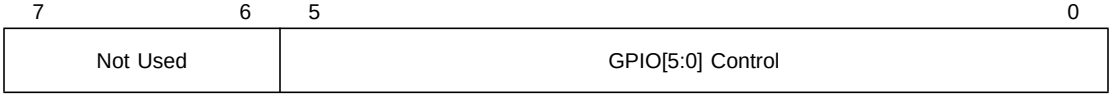
Not Used (0x0F) 7

Video Horizontal Active Bits [10:8] (0x0F) R/W 6:4
This register contains the upper three bits of the 11-bit Horizontal Active parameter. The contents of this register is concatenated with the contents of Register 0x0E to form the full value of this parameter.

Not Used (0x0F) 3

Video Horizontal Delay Bits [10:8] (0x0F) R/W 2:0
This register contains the upper three bits of the 11-bit Horizontal Delay parameter. The contents of this register is concatenated with the contents of Register 0x0D to form the full value of this parameter.

3.3.12 GPIO Control Register (0x10)



This register controls the GPIO[5:0] data pins. The bits that are set in this register correspondingly enable the output of the data that has been loaded into the GPIO Pins Register (0x11). The bits that are cleared in this register 3-state their corresponding GPIO pins.

Not Used 7:6

GPIO5 Control R/W 5
Setting this bit enables the output of bit 5 in register 0x11 across the GPIO5 signal (pin 85). Clearing this bit 3-states pin 85.

GPIO4 Control **R/W 4**
Setting this bit enables the output of bit 4 in register 0x11 across the GPIO4 signal (pin 137). Clearing this bit 3-states pin 137.

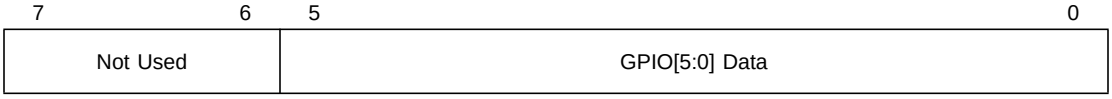
GPIO3 Control **R/W 3**
Setting this bit enables the output of bit 3 in register 0x11 across the GPIO3 signal (pin 133). Clearing this bit 3-states pin 133.

GPIO2 Control **R/W 2**
Setting this bit enables the output of bit 2 in register 0x11 across the GPIO2 signal (pin 116). Clearing this bit 3-states pin 116.

GPIO1 Control **R/W 1**
Setting this bit enables the output of bit 1 in register 0x11 across the GPIO1 signal (pin 115). Clearing this bit 3-states pin 115.

GPIO0 Control **R/W 0**
Setting this bit enables the output of bit 0 in register 0x11 across the GPIO0 signal (pin 114). Clearing this bit 3-states pin 114.

3.3.13 GPIO Pins Register (0x011)



This register contains GPIO data. When the respective bits in the GPIO Control Register (0x10) are set, the GPIO[5:0] Data in this register is sent to the corresponding GPIO[5:0] pins. This register can be read to determine the status of the GPIO[5:0] pins.

Not Used **7:6**

GPIO5 Data **R/W 5**
This bit contains data from/to the GPIO5 signal (pin 85). When bit 5 in register 0x10 is set, the value of this bit is output to GPIO5.

GPIO4 Data **R/W 4**
This bit contains data from/to the GPIO4 signal (pin 137). When bit 4 in register 0x10 is set, the value of this bit is output to GPIO4.

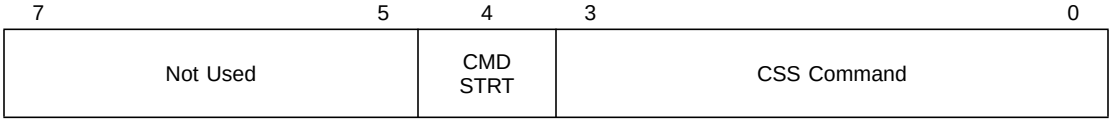
GPIO3 Data **R/W 3**
This bit contains data from/to the GPIO3 signal (pin 133). When bit 3 in register 0x10 is set, the value of this bit is output to GPIO3.

GPIO2 Data **R/W 2**
This bit contains data from/to the GPIO2 signal (pin 116). When bit 2 in register 0x10 is set, the value of this bit is output to GPIO2.

GPIO1 Data **R/W 1**
This bit contains data from/to the GPIO1 signal (pin 115). When bit 1 in register 0x10 is set, the value of this bit is output to GPIO1.

GPIO0 Data **R/W 0**
This bit contains data from/to the GPIO0 signal (pin 114). When bit 0 in register 0x10 is set, the value of this bit is output to GPIO0.

3.3.14 CSS Command Register (0x12)



Not Used **7:5**

CMDSTRT **Command Start** **R/W 4**
????

CSSCMD **CSS Command** **R/W 3:0**

This field contains the current CSS command. The CSS commands are listed as follows:

Bits 3:0	Command Name	Description
0000	HstCmdNone	???
0001	HstCmdPassThru	???
0101	HstCmdDescram	???
1000	HstCmdGenCh	???
1001	HstCmdRdCh	???
1010	HstCmdWrCh	???
1011	HstCmdWrDrvRef	???
1100	HstCmdDrvAuth	???
1101	HstCmdDecAuth	???
1110	HstCmdDiscKey	???
1111	HstCmdTitleKey	???

3.3.15 CSS Status Register (0x13)

7	2	1	0
Not Used		CSS Success	CSS Running

This register contains CSS status information.

Not Used **7:2**

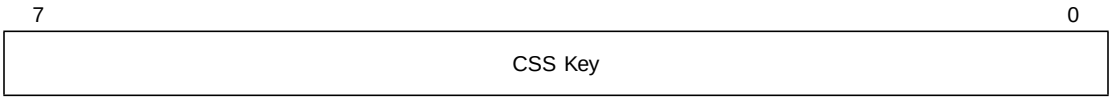
CSS Success **R/W 1**

When set, this bit indicates that CSS descrambling was successful.

CSS Running **R/W 0**

When set, this bit indicates that the CSS descrambling process is currently running. When it is cleared, no CSS descrambling process is running.

3.3.16 CSS Key Register (0x14)

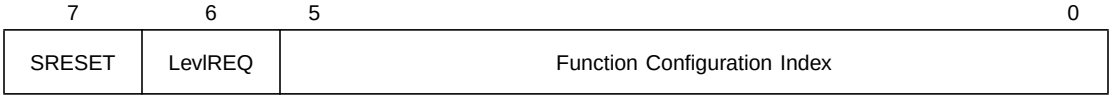


CSS Key **R/W 7:0**
This register holds the 8-bit disc/title key during CSS descrambling operations.

3.4 Configuration Option Register

The Configuration Option Register is located at offset 0 in the Attribute Memory Space. This host uses this register to configure the PC Card, to control its interrupts, and to control a soft reset of the card. The Configuration Option Register is required for PC Cards that use the I/O interface.

3.4.1 Configuration Option Register (Attribute Memory, Offset 0)



SRESET **Soft Reset** **R/W 7**
By setting this bit, the host can soft reset the PC Card. When the host clears this bit after a soft reset, the PC Card enters the same state as it would following a hard reset or power-up. Clearing this bit also clears bits 5:0 in this register.

LevlREQ **Level Mode Interrupt Request** **R/W 6**
When this bit is set, the PC Card will generate Level Mode interrupts. When this bit is cleared, the PC Card will generate Pulse Mode interrupts (if supported). For more details, refer to the *PC Card Standard* documentation.

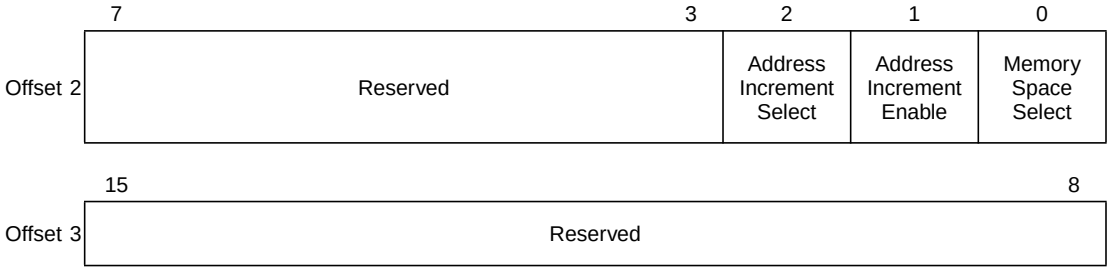
Function Configuration Index **R/W 5:0**
The values in this field correspond to PC Card functions as they are defined by a Configuration Table Entry Tuple (see *PC Card Standard* documentation.) These bits are

cleared when the host issues a soft or hard reset. While these bits are zero, the PC Card uses the Memory Only interface and ignores all I/O cycles from the host. Regardless of the interface in use, the CIS must be readable according the *PC Card Standard Metaformat Specification.*

3.5 Indirect Access Registers

The Indirect Access Registers are located at offsets 2 through 9 in the Common Memory Space. This set of registers provides control for indirect addressing of data in the Attribute and Common Memory spaces. The indirect access mechanism requires only four address lines (HA[3:0]) to access these memory spaces. The size of the access spaces is 512 x 8 bits.

3.5.1 Indirect Access Control Register (Common Memory, Offset 2-3)



The 16-bit Indirect Access Control Register controls the addressing of data in the Attribute and Common Memory spaces for indirect read and write operations. The lower 8 bits [7:0] of this register are located at offset 2 in the Common Memory Space. The upper 8 bits [15:8] of this register are located at offset 3. All reserved bits must be cleared.

Reserved (set to zero) **15:3**

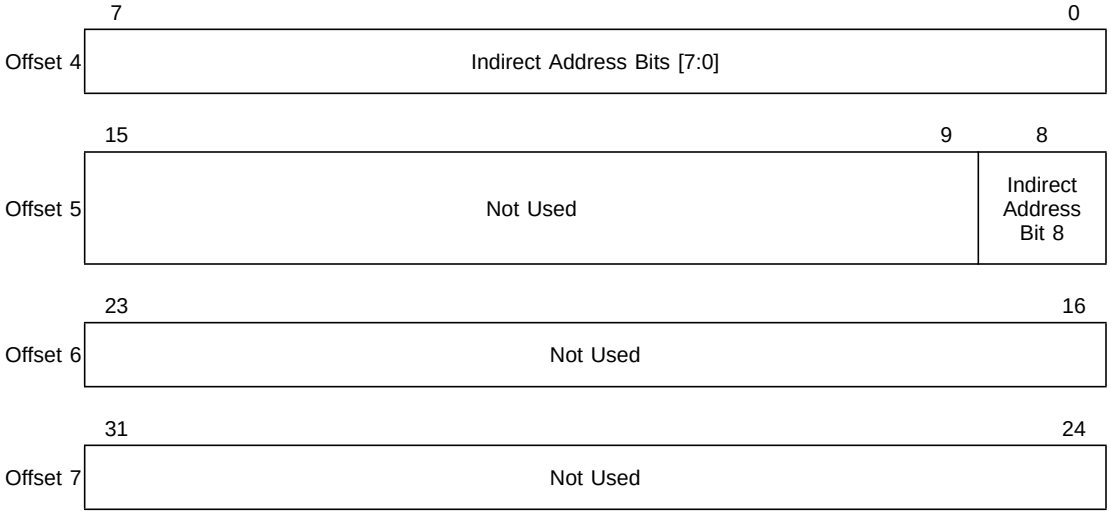
Address Increment Select **R/W 2**
When the host sets this bit, the indirect address value is incremented by two after each data read/write access. When the host clears this bit, the indirect address value is incremented by one after each data read/write access.

Bit 1 of this register must be set to enable automatic address incrementation.

Address Increment Enable **R/W 1**
When set, this bit enables automatic address incrementation according the amount specified in bit 2 of this register.

Memory Space Select **R/W 0**
Setting this bit, enables indirect access to the Common Memory Space. Clearing this bit, enables indirect access to the Attribute Memory Space.

3.5.2 Indirect Access Address Register (Common Memory, Offset 4-7)

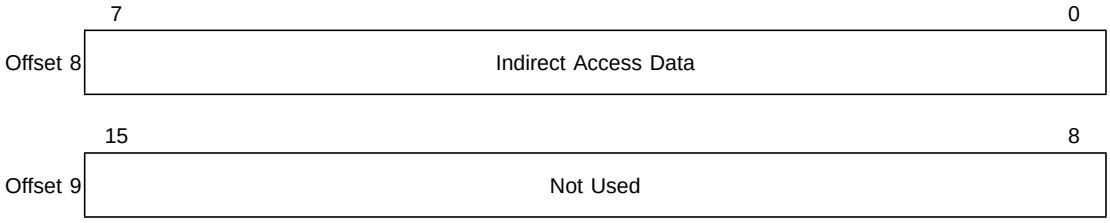


Not Used (set to zero) **31:9**

Indirect Address [8:0] **R/W 8:0**
This register indicates the current 9-bit address that will be used for the next data read/write access. Since the address is 9 bits, only bits [8:0] in this register are used. All other bits must be cleared. The host adjusts the value of this address and selects the memory space to be addressed by writing to the Indirect Access Control Register (offset 2-3).

Indirect Address Bits [7:0] are located at offset 4 in the Common Memory Space. Indirect Address Bit 8 is located at offset 5.

3.5.3 Indirect Access Data Register (Common Memory, Offset 8-9)



Not Used **15:8**

Indirect Access Data **R/W 7:0**
Reading this register fetches the 8-bit data that is located at the address specified in the Indirect Access Address Register (offset 4-7) within the memory space that is selected in the Indirect Access Control Register (offset 2-3). When reading from an address in the Attribute Memory Space, only the even byte data is valid. When reading from an address in the Common Memory Space, both even and odd bytes are valid.

Writing to this register sends 8-bit data to the address specified in the Indirect Access Address Register (offset 4-7) within the memory space that is selected in the Indirect Access Control Register (offset 2-3).

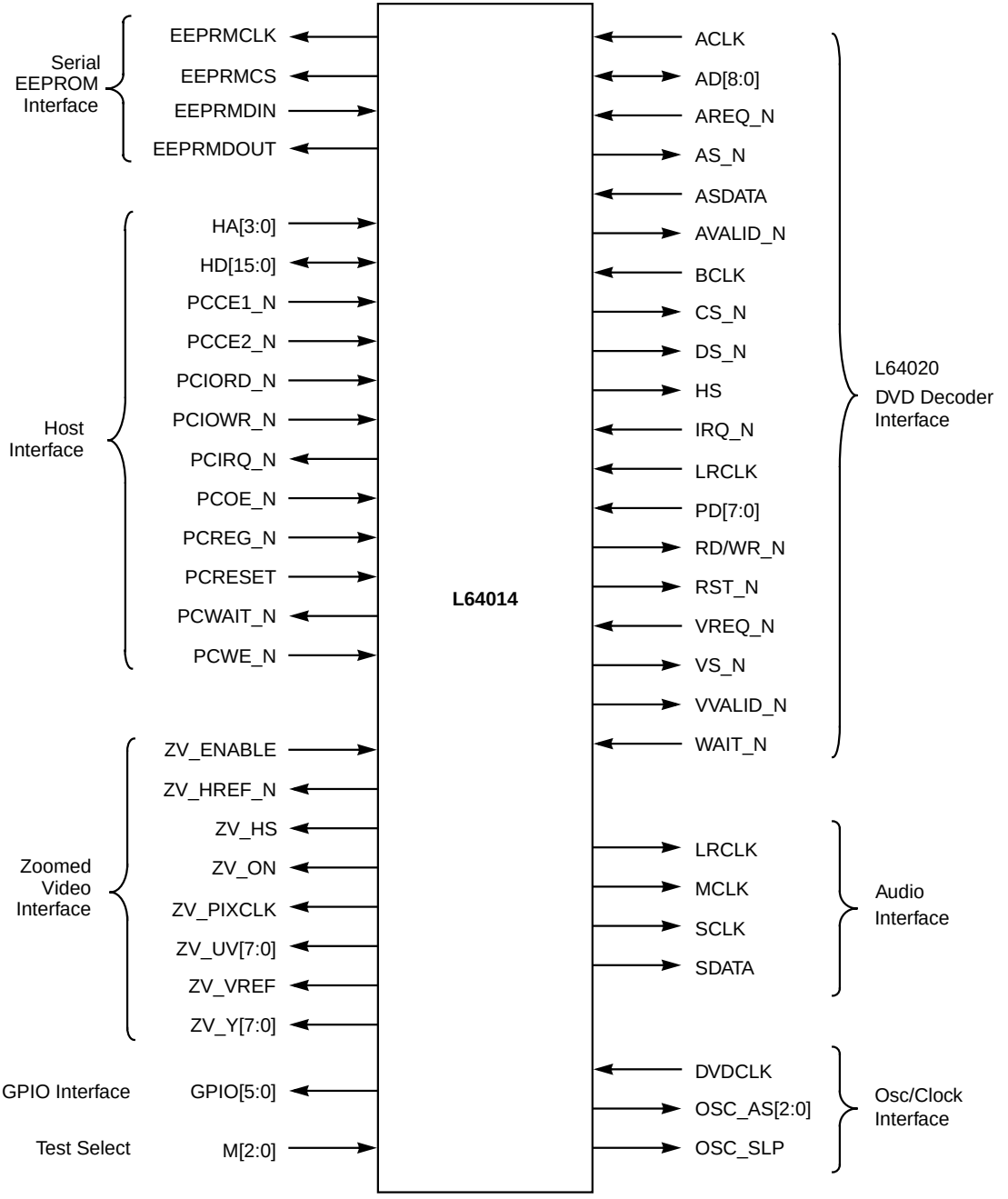
Chapter 4
Signals

This chapter describes the L64014 input/output signals and includes the following sections:

4.1 Signals Groups

The L64014 signals are divided into eight groups. Figure 4.1 shows the signal groups, the individual signal names, and their input/output direction. Signal names ending with “_N” indicate an active-LOW signal. All other signals are active HIGH.

Figure 4.1 L64014 I/O Signal Diagram



4.2 Audio Interface

The Audio interface outputs I^2S formatted digital audio data and audio clock signals to the ZV port.

LRCLK **Audio Left/Right Clock** **Output**
This clock signal enables the left or right serial data output. When this signal is asserted, the right audio channel is enabled. Deasserting this signal enables the left audio channel.

MCLK **Audio Master Clock** **Output**
This signal is the digital audio master clock. This clock runs at the same frequency as the DVD decoder's audio master clock (ACLK) signal.

SCLK **Audio Serial Clock** **Output**
This signal is the serial audio digital PCM clock.

SDATA **Audio Serial Data** **Output**
This signal is the digital audio serial data output. The format of this signal is controlled by writing to bit 4 in the Oscillator and Audio Control Register (0x08),

4.3 Serial EEPROM Interface

The EEPROM Control Register (0x0C) drives the EEPROM interface signals.

EEPRMCLK **EEPROM Clock** **Output**
This is the clock output to the external EEPROM. Bit 1 in the EEPROM Control Register (0x0C) controls this clock.

EEPRMCS **EEPROM Chip Select** **Output**
Asserting this signal enables the external EEPROM for read/write operations. Bit 0 in the EEPROM Control Register (0x0C) controls this signal.

EEPRMDOUT **Data to EEPROM** **Output**
This signal supplies serial data output to the external EEPROM. Bit 2 in the EEPROM Control Register (0x0C) controls this signal.

EEPRMDIN **Data from EEPROM** **Input**
This signal receives serial data input from the external EEPROM. Bit 3 in the EEPROM Control Register (0x0C) controls this signal.

4.4 Host Interface

HA[3:0] **Host Address [3:0]** **Input**
This 4-bit address bus provides host access to the L64014's internal registers.

HD[15:0] **Host Data [15:0]** **I/O**
These lines provide a 16-bit bidirectional host data bus. HD15 is the most significant bit.

PCCE1_N **PC Card Enable 1** **Input**
Asserting this signal (LOW) enables even numbered address bytes.

PCCE2_N **PC Card Enable 2** **Input**
Asserting this signal (LOW) enables odd number address bytes.

PCIORD_N **PC I/O Read** **Input**
The host asserts this signal (LOW) to read data from the PC Card's I/O registers. The PC Chip Enable 1 or 2 signals must also be asserted to enable read operations.

PCIOWR_N **PC I/O Write** **Input**
The host asserts this signal (LOW) to write data to the PC Card's I/O registers. The PC Chip Enable 1 or 2 signals must also be asserted to enable write operations. Until the L64014 has been configured for I/O operations, it will not respond to this signal.

PCIRQ_N **PC Interrupt Request** **Output**
The L64014 asserts this signal (LOW) to indicate to the host that the PC Card requires service.

PCOE_N **Output Enable** **Input**
When this signal is LOW, it enables memory read data.

PCREG_N **PC Reg** **Input**
When the host asserts this signal (LOW), access is limited to the Attribute Memory Space and the I/O Address Space. The Attribute Memory Space contains card configuration and attribute information. I/O Address Space provides access to peripheral devices.

PCRESET **PC Reset** **Input**
This signal initializes all L64014 registers and returns the L64014 to its original unconfigured state.

PCWAIT_N **PC Wait** **Output**
The L64014 asserts this signal (LOW) to delay the completion of the current memory or I/O access cycle.

PCWE_N **Memory Write Enable** **Input**
When this signal is asserted (LOW), it enables PC Card write operations. This includes write access to the Configuration Option and Indirect Access registers.

4.5 GPIO Interface

GPIO[5:0] **General Purpose I/O [5:0]** **I/O**
These general purpose data lines are controlled and read by the GPIO Control Register (0x10) and the GPIO Pins Register (0x11), respectively.

4.6 L64020 DVD Decoder Interface

ACLK **Decoder Audio Master Clock** **Input**
This signal is the audio output clock from the DVD Decoder.

AD[8:0] **Decoder Address/Data [8:0]** **I/O**
These lines function as a 9-bit host address bus (AS[8:0]), an 8-bit host data bus (AS[7:0]), or an 8-bit channel data bus (AS[7:0]).

AS[7:0] serves as an 8-bit host data bus to program the DVD decoder and to access decoder status and bitstream information. During read cycles, the WAIT_N signal indicates when bus data is valid. During write cycles,

the host data latches in the Decoder on the rising edge of the DS_N signal.

AS[7:0] functions as an 8-bit channel data bus for porting parallel MPEG bitstreams to the DVD Decoder.

ASDATA

Decoder Audio Serial Data **Input**
This signal receives serial digital audio data from the L64020 DVD A/V Decoder.

AREQ_N **Decoder Audio Request** **Input**
The L64020 asserts AREQ_N (LOW) when it is ready to receive a new byte of coded audio data from a transport stream demultiplexer while in the A/V PES mode, or a new byte of any data while in the PS mode.

AS_N **Decoder Address Strobe** **Output**
When the L64014 asserts this signal (LOW), the DVD decoder latches the address.

AVALID_N **Decoder Audio Valid** **Output**
In response to an active AREQ_N signal from the DVD decoder, L64014 asserts this signal (LOW) when it has placed a valid data byte on the channel data bus AD[7:0]. The DVD decoder reads the byte of data when the L64014 deasserts AVALID_N (HIGH).

BCLK **Decoder Audio Bit Serial Clock** **Input**
The L64014 uses this signal to clock-in the PCM serial audio data from the DVD decoder.

CS_N **Decoder Chip Select** **Output**
The L64014 asserts this signal to access the L64020 DVD A/V Decoder chip for read/write operations. CS_N must remain LOW during the entire read/write cycle.

DS_N **Decoder Data Strobe** **Output**
The L64014 asserts this signal (LOW) to strobe data in or out of the L64020 DVD A/V Decoder.

HS **Decoder Horizontal Sync** **Output**
HS is the horizontal sync signal to the DVD decoder and to the NTSC/PAL video encoder. HS is synchronous to the DVDCLK signal.

IRQ_N **Decoder Interrupt Request** **Input**
The L64020 asserts this active-LOW signal to tell the L64014 that an unmasked interrupt condition has occurred in the DVD decoder. The host must read registers 0 through 4 in the L64020 DVD A/V Decoder to determine the cause of the interrupt. Once the host completes the appropriate action, it must set bit 0 in Register 6 of the L64020 to deassert IRQ_N (HIGH).

LRCLK **Decoder Audio Left/Right Clock** **Input**
This signal indicates which samples presented on the ASDATA pin belong to the left and right stereo audio channels. To comply with PC Card ZV port standards, LRCLK is driven HIGH when the ASDATA pin presents a right audio channel sample, and LRCLK is driven LOW when the ASDATA pin presents a left audio channel sample.

PD[7:0] **Decoder Pixel Data [7:0]** **Input**
The PD[7:0] bus, which is input from the DVD decoder, carries the pixel data for the reconstructed video. The pixel data is in YCbCr format in accordance with ITU-R BT.601 standards.

RD/WR_N **Decoder Read (HIGH) / Write (LOW)** **Output**
The L64014 drives this signal HIGH for DVD decoder read cycles, and drives it LOW for DVD decoder write cycle. CS_N must remain LOW during an entire read/write cycle.

RST_N **Decoder Reset** **Output**
Bit 0 in the LSI Control Register (0x06) controls this signal. When the L64014 asserts RST_N (LOW), the L64020 initializes its internal MCU, FIFO controllers, state machines, and registers. The minimum reset pulse width is eight DVDCLK (27 MHz) cycles, which equals 300 ns. Both DVDCLK and ACLK must be running during reset.

VREQ_N **Decoder Video Request** **Input**
The DVD decoder asserts VREQ_N when it is ready to receive a new byte of coded video data in A/V PES mode. VREQ_N is not used in PS mode.

VS_N **Decoder Vertical Sync** **Output**

VS_N is the vertical sync signal to both the DVD decoder and the NTSC/PAL video encoder. By writing to bit 0 in the Video Control 0 register (0x09), the host can designate this signal as either a conventional vertical sync input or an even/odd field indicator. In the Even/Odd Field Indicator mode, bit 1 of the Video Control 0 register controls the polarity of the even/odd fields. VS_N is synchronous to DVDCLK.

VVALID_N **Decoder Video Valid** **Output**

In response to a VREQ_N signal from the L64020, the L64014 asserts this signal (LOW) once it has placed a valid data byte on the AD[7:0] channel data bus. The L64020 inputs the byte of video data after it deasserts VREQ_N.

WAIT_N **Decoder Wait** **Input**

The L64020 asserts WAIT_N (LOW) to indicate that its host interface is busy with a read or write cycle. It deasserts WAIT_N (HIGH) when the current cycle is completed. WAIT_N is 3-stated when CS_N is HIGH.

4.7 Test Select

M[2:0] **Test Select [2:0]** **Input**

The test select signals enable either normal operation or one of the test modes as shown in the following table:

M2	M1	M0	Function
L	H	L	Normal PC Card operation
H	H	L	3-state output test
H	H	H	Scan flip-flop test

4.8 Oscillator and Clock Interface

DVDCLK **27-MHz Clock** **Input**
This clock is the 27-MHz system clock from an external oscillator.

OSC_AS[2:0] **Audio Oscillator Frequency Set Bits [2:0]** **Output**
These signals are output to the oscillator and select the audio master clock frequency. The OSC_AS[2:0] signals correspond directly to the AFS2:0 bits in the Oscillator and Audio Control Register (0x08).

OSC_SLP **Oscillator Sleep** **Output**
When the L64014 asserts this signal, it forces the external oscillator into Sleep mode. The Oscillator and Audio Control Register (0x08) controls this signal. Bit 3 of this register is used to disable external oscillators.

4.9 Zoomed Video Interface

ZV_ENABLE **Zoomed Video Enable** **Input**
When HIGH, this signal enables the output to the Zoomed Video port. When LOW, this signal 3-states the ZV port. This signal can be used only when bits 7 and 6 in the Video Control 1 Register (0x0A) are set to 1 and 0, respectively.

ZV_HREF_N **Zoomed Video Horizontal Reference** **Output**
This signal provides horizontal sync. The three ZV Horizontal Reference Control Registers (0x0D, 0x0E, and 0x0F) control the parameters that program this signal. The Video Control 1 Register (0x0A) controls the polarity of this signal.

ZV_ON **Zoomed Video On** **Output**
This signal is HIGH when the L64014 drives the Zoomed Video outputs; it is LOW when the ZV outputs are 3-stated.

ZV_PIXCLK **Zoomed Video Pixel Clock** **Output**
This signal provides the selectable, 13.5-MHz or 27-MHz, ZV pixel clock. By writing to bit 2 in the Video Control 0 Register (0x09), the host can select the clock frequency.

ZV_VREF **Zoomed Video Vertical Reference** **Output**
This signal provides vertical sync. The Video Control 1 register (0x0A) controls the polarity of this signal.

ZV_UV[7:0] **Zoomed Video Chroma Bit(7:0)** **Output**
In 16-bit mode, these lines output 8 bits of UV chrominance data to the ZV port. These signals are not used in 8-bit mode. The host can select the 16-bit mode by setting bit 4 in the Video Control 0 Register (0x09).

ZV_Y[7:0] **Zoomed Video Luma Bit(7:0)** **Output**
In 16-bit mode, these lines output 8 bits of Y luminance data to the ZV port. In 8-bit mode, these signals carry 8 bits of YUV pixel data. The host can select the 16-bit mode by setting bit 4 in the Video Control 0 Register (0x09).

ZV_HS **Zoomed Video Horizontal Sync** **Output**
The ZV port does not use this signal. It has the same pulse width and frequency as the DVD decoder HS signal.

Chapter 5
Specifications

This chapter provides the electrical and mechanical specifications for the L64014 chip. This information is organized in the following sections:

Section 5.1 includes electrical specifications for the L64014, such as absolute maximum ratings, recommended operating conditions, and DC characteristics. Section 5.2 includes AC timing specifications on the L64014 interfaces. The “Pin Summary” section includes a pinout diagram for the L64014, as well as an alphabetical list of its signal names and their corresponding pin numbers. Section 5.4 presents the mechanical drawings for the 144-pin TQFP package, which houses the L64014.

5.1 Electrical Requirements

This section specifies the electrical requirements for the L64014. Four tables list electrical data in the following categories:

- Absolute Maximum Ratings (Table 5.1)
- Recommended Operating Conditions (Table 5.2)
- Capacitance (Table 5.3)
- DC Characteristics (Table 5.4)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Unit
V_{DD}	DC Supply	–0.3 to +3.9	V
V_{IN}	5 V Compatible Input Voltage	–1.0 to 6.5	V
I_{IN}	DC Input Current	±10	µA
T_{STG}	Storage Temperature Range, Plastic	–40 to +125	°C

1. Referenced to V_{SS}.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply, Commercial	+3.0 to +3.6[1]	V
T_A	Operating Ambient Temperature	0 to +70	°C
T_J	Junction Temperature	≤150	°C

1. For the L64020, the recommended DC supply voltage range is +3.14 V to +3.46 V.

Table 5.3 Capacitance

Symbol	Parameter[1]	Min	Typ	Max	Unit
C_{IN}	Input Capacitance (5 V compatible)		3.0		pF
C_{OUT}	Output Capacitance		3.0		pF
C_{IO}	I/O Bus Capacitance		3.0		pF

1. Measurement conditions are V_{IN} = 3.3 V, T_A = 25 ˚C, and clock frequency = 1 MHz.

Table 5.4 DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IL}	Voltage Input Low		V_{SS} – 0.5	–	0.8	V
V_{IH}	Voltage Input High	5-V compatible	2.0	–	5.5	V
V_T	Switching Threshold			1.4	2.0	V
V_{OH}	Voltage Output High	I_{OH} = –4.0 mA	2.4	–	V_{DD}	V
V_{OL}	Voltage Output Low	I_{OL} = 4.0 mA I_{OL} = 6.0 mA (GPIO[5:0])	–	0.2	0.4	V
I_{IN}	Input Current	V_{IN} = V_{DD} or V_{SS}	–10	±1	10	µA
I_{OZ}	Current 3-State Output Leakage	V_{OUT} = V_{SS} or V_{DD}	–10	±1	10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}	TBD	TBD	TBD	µA
I_{CC}	Dynamic Supply Current	V_{DD} = Max, f = 27 MHz DVDCLK	–	TBD	–	mA

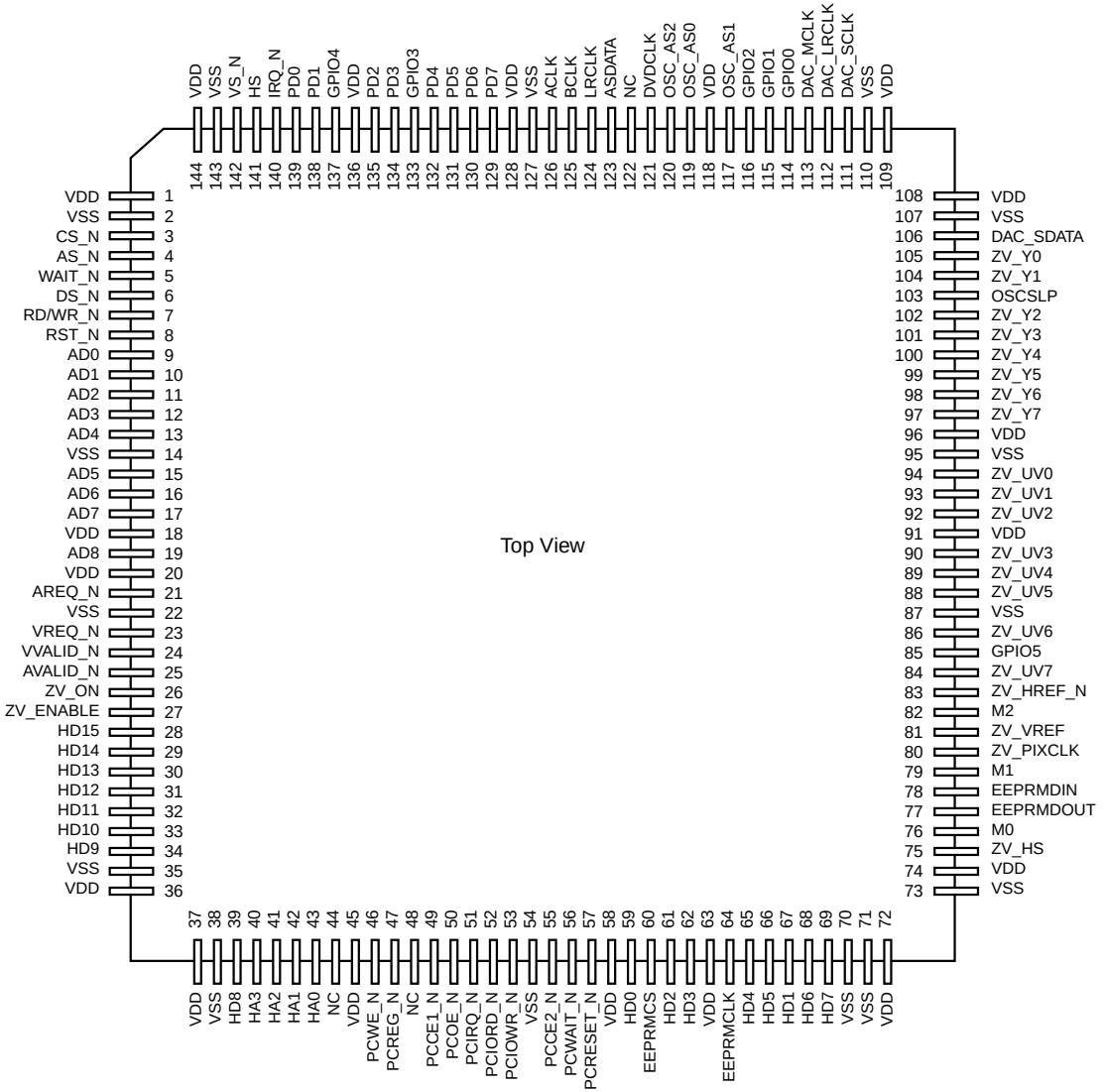
1. Junction temperature range: 0 to 115 °C, ± 5% power supply.

5.2 AC Timing

TBD

5.3 Pin Summary

Figure 5.1 144-pin TQFP Pinout



1. *NC* pins are not connected.

Table 5.5 Alphabetical Pin List for the 144-pin TQFP Package

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ACLK	126	GPIO5	85	OSC_AS1	117	VDD	20
AD0	9	HA0	43	OSC_AS2	120	VDD	36
AD1	10	HA1	42	OSCSLP	103	VDD	37
AD2	11	HA2	41	PCCE1_N	49	VDD	45
AD3	12	HA3	40	PCCE2_N	55	VDD	58
AD4	13	HD0	59	PCIORD_N	52	VDD	63
AD5	15	HD1	67	PCIOWR_N	53	VDD	72
AD6	16	HD2	61	PCIRQ_N	51	VDD	74
AD7	17	HD3	62	PCOE_N	50	VDD	91
AD8	19	HD4	65	PCREG_N	47	VDD	96
AREQ_N	21	HD5	66	PCRESET_N	57	VREQ_N	23
AS_N	4	HD6	68	PCWAIT_N	56	VS_N	142
ASDATA	123	HD7	69	PCWE_N	46	VSS	107
AVALID_N	25	HD8	39	PD0	139	VSS	110
BCLK	125	HD9	34	PD1	138	VSS	127
CS_N	3	HD10	33	PD2	135	VSS	14
DAC_LRCLK	112	HD11	32	PD3	134	VSS	143
DAC_MCLK	113	HD12	31	PD4	132	VSS	2
DAC_SCLK	111	HD13	30	PD5	131	VSS	22
DAC_SDATA	106	HD14	29	PD6	130	VSS	35
DS_N	6	HD15	28	PD7	129	VSS	38
DVDCLK	121	HS	141	RD/WR_N	7	VSS	54
EEPRMCLK	64	IRQ_N	140	RST_N	8	VSS	70
EEPRMCS	60	LRCLK	124	VDD	1	VSS	71
EEPRMDIN	78	M0	76	VDD	108	VSS	73
EEPRMDOUT	77	M1	79	VDD	109	VSS	87
GPIO0	114	M2	82	VDD	118	VSS	95
GPIO1	115	NC	122	VDD	128	VVALID_N	24
GPIO2	116	NC	44	VDD	136	WAIT_N	5
GPIO3	133	NC	48	VDD	144	ZV_ENABLE	27
GPIO4	137	OSC_AS0	119	VDD	18	ZV_HREF_N	83

(Sheet 1 of 2)

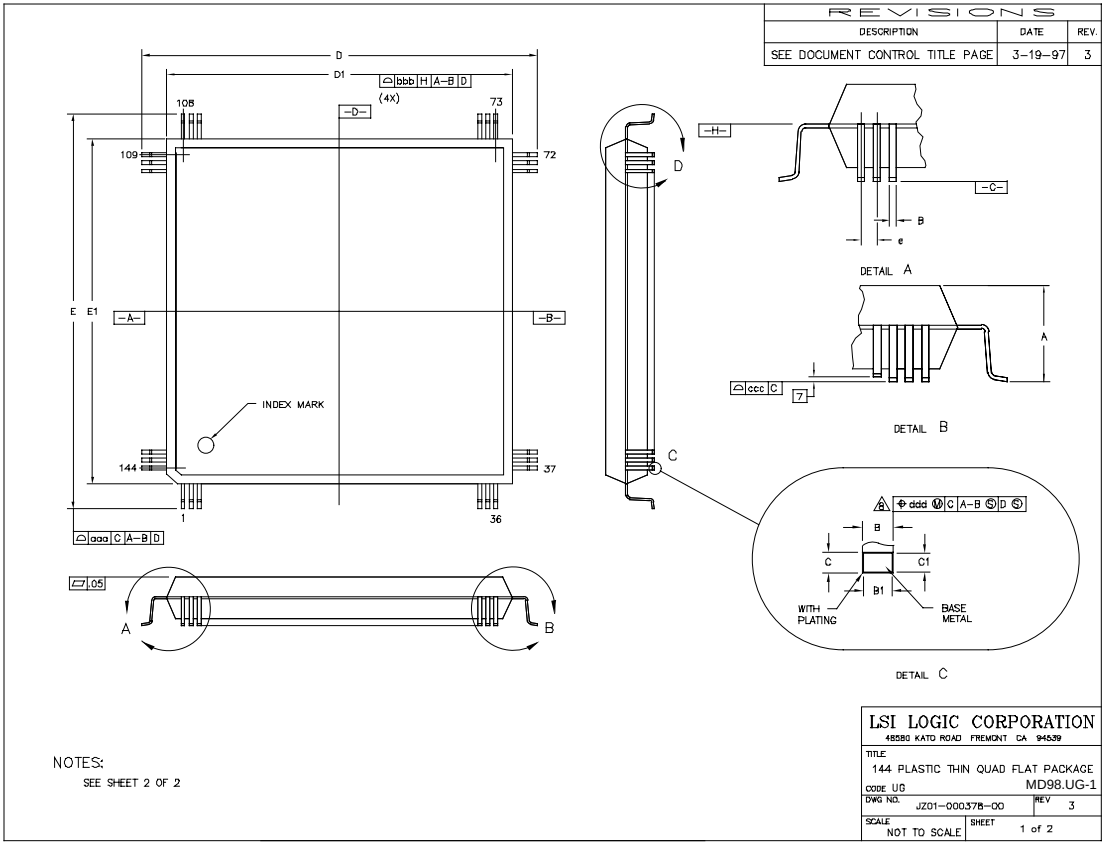
Table 5.5 (Cont.) Alphabetical Pin List for the 144-pin TQFP Package (Cont.)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ZV_HS	75	ZV_UV2	92	ZV_UV7	84	ZV_Y3	101
ZV_ON	26	ZV_UV3	90	ZV_VREF	81	ZV_Y4	100
ZV_PIXCLK	80	ZV_UV4	89	ZV_Y0	105	ZV_Y5	99
ZV_UV0	94	ZV_UV5	88	ZV_Y1	104	ZV_Y6	98
ZV_UV1	93	ZV_UV6	86	ZV_Y2	102	ZV_Y7	97

(Sheet 2 of 2)

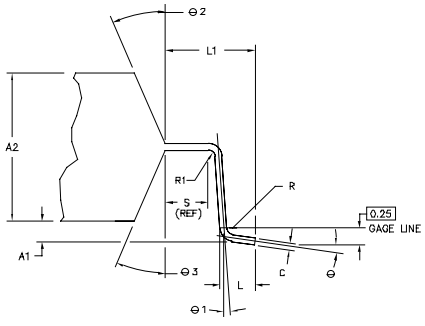
5.4 Packaging

Figure 5.2 144-pin TQFP (UG) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UG.**

Figure 5.2 144-pin TQFP (UG) Mechanical Drawing (Cont.)



DETAIL D

DIMENSIONS IN MM				
SYM	MIN	NOM	MAX	NOTE
A			1.60	
A1	0.05		0.15	
A2	1.35	1.40	1.45	
B	0.17	0.22	0.27	6, 10
B1	0.17	.20	0.23	
C	0.09	0.15	0.20	10
C1	0.09		0.16	
D	21.90	22.00	22.10	2
D1	19.90	20.00	20.10	3
e		0.5 BSC		8
E	21.90	22.00	22.10	2
E1	19.90	20.00	20.10	3
L	0.45	0.60	0.75	
L1		1.00		
N		144		
R	0.08	0.15	0.20	
R1	0.08			
S	0.20			
θ	0	3.5	7	
θ1	0			
θ2	11	12	13	
θ3	11	12	13	
aaa			0.20	
bbb			0.20	
ccc			0.08	
ddd			0.10	11

NOTES: UNLESS OTHERWISE SPECIFIED

1 DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF LEAD, WHERE THE LEAD EXITS THE PLASTIC BODY.

2 TO BE DETERMINED AT SEATING PLANE -C-

3 DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTUSION. ALLOWABLE PROTUSION IS .25mm PER SIDE.

4 THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-.

5 ALL DIMENSIONS IN MILIMETERS. CONTROLLING DIMENSION IN MILIMETER. INCHES SHALL BE ROUNDED TO NEAREST .001 INCH.

6 DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT MINIMUM SPACE BETWEEN ADJACENT LEADS TO BE 0.07mm.

7 COPLANARITY OF ALL LEADS SHALL BE WITHIN 0.08mm DIFFERENCE BETWEEN HIGHEST AND LOWEST LEAD WITH SEATING PLANE -C- AS REFERENCE.

8 LEAD PITCH DETERMINED AT DATUM -H-.

9 MARKING AREA FREE OF PROTRUSION AND INTRUSION

10 PLATING THICKNESS INCLUDED. PLATING THICKNESS TO BE 0.005 mm MIN; 0.020 mm MAX.

11 FROM TRUE LEAD LOCATION MEASURED AT SEATING PLANE -C-.

12 DATUM -A-, -B- AND -D- DETERMINE CENTERLINE OF LEADFRAME.

LSI LOGIC CORPORATION 48580 KATO ROAD FREMONT CA 94539		
TITLE: 144 PLASTIC THIN QUAD FLAT PACKAGE		
CODE UG	MD98.UG-2	
DWG NO JZ01-000378-00	REV. 3	
SCALE NOT TO SCALE	SHEET 2 of 2	

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UG.**

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