3.4 ROM EMULATOR POD (figures 3.7 and 3.8) PM 8864

The ROM emulator pod can only be used in conjuntion with the RS232C control card. The pod connects to this card via one 15-pole connector (refer also to figure 1.2 : PM 3632 block diagram).
The RS232C control card is used for transferring data from the mainframe to the ROM emulator pod via a serial link (not the RS232C connection!).
It also generates the necessary control signal for the ROM emulator pod.
The RS232C control card is also used for uploading or downloading of data from or to the ROM emulator pod. This is done via the RS232C serial link (in hex format).

The ROM emulator pod can emulate up to 16 K byte of PROM (2716, 2732, 2764, 27128). Two pods can be daisy chained in which case a total of 32 K bytes of PROM can be emulated.
Each pod contains eight 2K RAMs.

The ROM emulator pod is connected to the RS232C control card via connector P1 (see figure 3.7).
Via this connector, the RS232C C card can pass some control signals to the pod (under control of the microprocessors):

- BCLK (buffered clock): clock signal for filling the input buffers in the pod or for shifting data out of the input buffers to the RS232C control card.
- BCTL0,1 (buffered control lines): set the pod in read write or emulation mode.
- SELECT (pod select) : two lines are used to select one of the two ROM emulator pods.

Via this connector, the RS232C C control card can write data into the RAMs in the pod via a serial link (BDDWN; buffered data down) or read data out of the RAMs via a serial link (SELDAT; selected data (up)).
All signals can go to a second pod also, via connector P2, which can be connected to connector P1 of the second pod also. An exception is the serial data that goes up to the RS232C card, which can be from the first or the second pod.

Write data into the RAMs:
The serial data (1 byte) + addres (2 bytes) come in via line BDDWN (buffered data down) and is clocked into shift register U9, U17 and U18 on clock pulse BCLK (buffered clock). During this, signal RDMOD* (read mode) puts the register in the shift right mode, and signal INTL* (internal mode) enables the outputs.
When the data + addresses are available in parallel, signals IA11, IA12 and IA13 (internal address lines) are decoded to select one of the 8 RAMs (via decoder U8, see figure 3.8) which causes a write of the data to the selected address in the RAM (signals IWE0...IWE7).

Read data out of RAMs:
The serial address 2 bytes is clocked into shift registers U9 and U17 on clock pulse BCLK (buffered clock) via line BDDWN (buffered data down). Control signals are the same as described above, and signals IA11, IA12 and IA13 are decoded to point out one of the eight RAMs (signals IOE0... IOE7:output enable via U7, see figure 3.8).

After this, the data on that address is loaded into U18 (LD0..LD8) and then shifted out in series on clock pulse BCLK into shift register U11.

Signal ISDAT (internal serial data) goes via U3 (see figure 3.8) to U12 where is is called SELDAT (selected data). SELDAT goes via the RS232C control card to the microprocessor.
In case a second pod is connected, the read-data from this pod (XSDAT) will go via U3 where it is called SELDAT via connector P1 to the RS232C control card.

Pod in emulation mode:
In this mode, the RAM are disconnected from the mainframe and are filled with the necessary data. The RAMs are now under control of the system under test.
For connection to the system under test, four connectors are available, labelled A, B, C and D.
The following table shows which connector can be used in the different modes.

label:	connector:	modes:
A	P3	2716, 2732, 2764, 27128
B	P4	2716, 2732, 27128
C	P5	2716, 2732, 2764
D	P6	2716, 2732

As shown above, a 2716 or 2732 can be plugged-in at any connector.
The target supplies addresslines, data lines, chip enables and output enables to the RAMs in the pod.

2716 in A or B: Only A is described here, because both are very similar.
The adresslines (XA0..XA10) are applied directly (via U24, U25) to both RAMs which are dedicated to connector A (U13 and U14). These buffers are only enabled in the emulation mode via signal EXTL*. When the target activates the chip enable and/or output enable signals (XCE* and XOE*):

1. multiplexers U26, U27 are enabled to transfer data from U13 to P3. This is done via signal XOEL0* (via U28, U29). The multiplexer is set in the correct direction by the microprocessor via signal MODE1 (low; see table in figure 3.8).
2. the output enable signals for the RAMs (IOE0 and IOE1) are generated via signal XEN1 which selects RAMs U13, U14 or RAMs U15, U16. Signal XEN1 goes to U2 to generate the correct output enable signals for the RAMs (via U7, see figure 3.8).
   XEN1 is always low for 2716 in A. XEN1 is high when 2716 in B is enabled.

2716 in C or D: Only C is described here, because both are very similar (see figure 3.8).
The address lines (XA0...XA10) are applied directly (via U24,U25) to both RAMs, which are dedicated to connector C (U20 and U21). When the target activates the chip enable and/or output enable signals (via pin 11 and 15 of P5):

1: Buffer U30 is enabled: the data bus of the system under test is connected to the RAM outputs.

2: The output enable signals for the RAMs (IOE4 an IOE5 are generated via signal XEN3 which selects either RAMs U20, U21 or RAMs U22, U23. Signal XEN3 goes to U2 to generate the correct output enable signals for the RAMs (via U7).
XEN3 is always low for 2716 in C. XEN3 is high when 2716 in D is enabled.

2732 in A, B, C or D: This mode of operation is exactly the same as the above described 2716 operation. The only differences is that addressline XA11 is used to make a selection between the upper or the lower 2 K of RAM which is dedicated to each connector.
This selection is done via U7 (see figure 2.9) which generates the correct output enable signals (IOE0...IOE7) for the RAMs.

2764 in A or C: This mode of operation is very similar to the 2716 in A operation.
The difference is that two extra address lines (XA11 and XA12) are used to select one of the 4 RAMs. This is done via the selection circuit U2, U7 and associated components (see figure 3.8).
Signals XEN1 and XEN3 are not used for RAM selection anymore.

27128 in A or B: This mode of operation is very similar to the 2716 in A or B operation.
The difference is that now three extra address lines (XA11, XA12, XA13) are used to select one of the 8 RAMs. This is done via the selection circuit U2, U7 and associated components (see figure 3.8).
Signals XEN1 and XEN3 are not used for RAM selection anymore.
Another difference is that when the data is read out of RAMs U20, U21, U22 or U23, multiplexers U26, U27 (see figure 3.7) are set to a different direction; the data that is now passed to the system under test comes from HD0...HD7.

RAM selection circuitry:

The output enable signals for the RAMs are generatad by U2, U7 and associated components.
This circuitry is controlled by control signal SCTL1, the mode selection (MODE) signals and some address lines from the system under test or the microcomputer in the mainframe (IA11, IA12, IA13 come from U24, U25).
Multiplexer U2 can be set to the 2716/2732 or the 2764/27128 modes, depending on the MODE0 and MODE1.

Mode selection signals:

As shown in the two tables in figure 3.8, the ROM emulator pod can operate in an internal or an emulation mode.
In the internal mode some control signals (SCTL) determine the action that has to be performed (read, write or hold & shift right).

The mode is stored in shift register U4 by clocking a data byte into this register on clock pulses BCLK (buffered clock) via the serial link (BDOWN; buffered data down). This however can only be done when the pod is selected (signal SELECT*).
The MODE signals select registers (U9, U7, U18) and the address buffers (U24, U25) via signals INTL*, EXTL*.
The control signals (BCTL0, BCTL1; come from U12) which drive multiplexer U3 determine which operation can be performed by the pod: read data or write data.

Pod connection errors:

If the pod is connected correctly to the system under test is detected by Q1 and associated components (connector A).
The microprocessor can read (via XSTS0A, XSTS0B; go to shift register U11) if the supply voltage (XPWR0) of the system under test is connected to the correct pin at connector A. If not, the analyzer will display "POD CONNECTION ERRROR" on the screen.
If it is connected in the correct way, FET Q1 will connect system ground to mainframe ground. If the connection is wrong, FET Q1, doesn't make that connection: The message POD CONNECTION ERROR will appear at the screen.

Reading pod identity.

When powering up the PM 3632, the microprocessor reads the identity of the ROM emulator pod by sending data to shift registers U9, U17, U18 via the serial link (BDDWN) on the RS232C control card, and afterwards read the same data back via shift register U11 and the same serial link (SELDAT).

LIST OF SIGNAL NAMES (diagram 14)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
BCLK	Buffered Rom emulator clock	14	14,15
BCTL0	Buffered control line 0	14	15
BCTL1	Buffered control line 1	14	15
BDDWN	Buffered data down	14	14,15
BSELDAT	Buffered serial data up	14	22
CTL0	Control line 0	22	14
CTL1	Control line 1	22	14
DDWN	Data down (to Rom emulator)	22	14
ECLK	Rom emulator clock	22	14
EXTL*	Select external (emulation) mode	15	14
HD0	Rom emulator data 0	15	14 BD
HD1	Rom emulator data 1	15	14 BD
HD2	Rom emulator data 2	15	14 BD
HD3	Rom emulator data 3	15	14 BD
HD4	Rom emulator data 4	15	14 BD
HD5	Rom emulator data 5	15	14 BD
HD6	Rom emulator data 6	15	14 BD
HD7	Rom emulator data 7	15	14 BD
IA 0	Addressline 0 (internal source)	14	15
IA 1	Addressline 1 (internal source)	14	15
IA 2	Addressline 2 (internal source)	14	15
IA 3	Addressline 3 (internal source)	14	15
IA 4	Addressline 4 (internal source)	14	15
IA 5	Addressline 5 (internal source)	14	15
IA 6	Addressline 6 (internal source)	14	15
IA 7	Addressline 7 (internal source)	14	15
IA 8	Addressline 8 (internal source)	14	15
IA 9	Addressline 9 (internal source)	14	15
IA10	Addressline 10 (internal source)	14	15
IA11	Addressline 11 (internal source)	14	15 ?
IA12	Addressline 12 (internal source)	14	15 ?
IA13	Addressline 13 (internal source)	14	14 ?
IA13	Addressline 13 (internal source)	14	14 ?
IA13	Addressline 13 (internal source)	14	15 ?
IOE0*	Output enable, (internal) RAM 0	15	14
IOE1*	Output enable, (internal) RAM 1	15	14
IOE2*	Output enable, (internal) RAM 2	15	14
IOE3*	Output enable, (internal) RAM 3	15	14
ISDAT	(internal) Serial data up	14	15
IWE0*	Write enable, (internal) RAM 0	15	14
IWE1*	Write enable, (internal) RAM 1	15	14
IWE2*	Write enable, (internal) RAM 2	15	14
IWE3*	Write enable, (internal) RAM 3	15	14
LD0	Rom emulator data 0	14	14,15 BD
LD1	Rom emulator data 1	14	14,15 BD
LD2	Rom emulator data 2	14	14,15 BD
LD3	Rom emulator data 3	14	14,15 BD
LD4	Rom emulator data 4	14	14,15 BD
LD5	Rom emulator data 5	14	14,15 BD
LD6	Rom emulator data 6	14	14,15 BD
LD7	Rom emulator data 7	14	14,15 BD
MODE 1	mode 1 select	15	14
ROMOD*	Select read mode	15	14

LIST OF SIGNAL NAMES (diagram 14, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
SEL0	Select line 0	22	14
SEL1	Select line 1	22	14
SELOAT	Serial data up (to mainframe)	15	14
SELECT*	Select line	14	15
STSLOD*	Load connection test data	15	14
VREF	Reference voltage (threshold)	14	12,13
XA 0	Addressline 0 (external source)	14,15	14 ?
XA 1	Addressline 1 (external source)	14,15	14 ?
XA10	Addressline 10 (external source)	14,15	14 ?
XA11	Addressline 11 (external source)	14,15	14 ?
XA12	Addressline 12 (external source)	14,15	14 ?
XA13	Addressline 13 (external source)	14,15	14 ?
XA 2	Addressline 2 (external source)	14,15	14 ?
XA 3	Addressline 3 (external source)	14,15	14 ?
XA 4	Addressline 4 (external source)	14,15	14 ?
XA 5	Addressline 5 (external source)	14,15	14 ?
XA 6	Addressline 6 (external source)	14,15	14 ?
XA 7	Addressline 7 (external source)	14,15	14 ?
XA 8	Addressline 8 (external source)	14,15	14 ?
XA 9	Addressline 9 (external source)	14,15	14 ?
XCE0*	Chip enable, port A (ext. source)	14	14
XCE1*	Chip enable, port B (ext. source)	14	14
XCOM0	Ground on port A (ext. source)	14	15
XCOM1	Ground on port B (ext. source)	14	15
XEN0	Select RAM for port A (ext.source)	14	not used
XEN1	Select RAM for port B (ext.source)	14	15
XOE0*	Output enable, port A (ext.source)	14	14
XOE1*	Output enable, port B (ext.source)	14	14
XOEL0*	Enable multiplexer output	14	14
XPWR0	Power on port A (ext. source)	14	15
XPWR1	Power on port B (ext. source)	14	15
XSDAT	Serial data up (from second pod)	14	15
XSEL	Select multiplexer direction	14	14
XSTS0A	Conection test, port A	15	14
XSTS0B	Conection test, port A	15	14
XSTS1A	Conection test, port B	15	14
XSTS1B	Conection test, port B	15	14
XSTS2A	Conection test, port C	15	14
XSTS2B	Conection test, port C	15	14
XSTS3A	Conection test, port D	15	14
XSTS3B	Conection test, port D	15	14

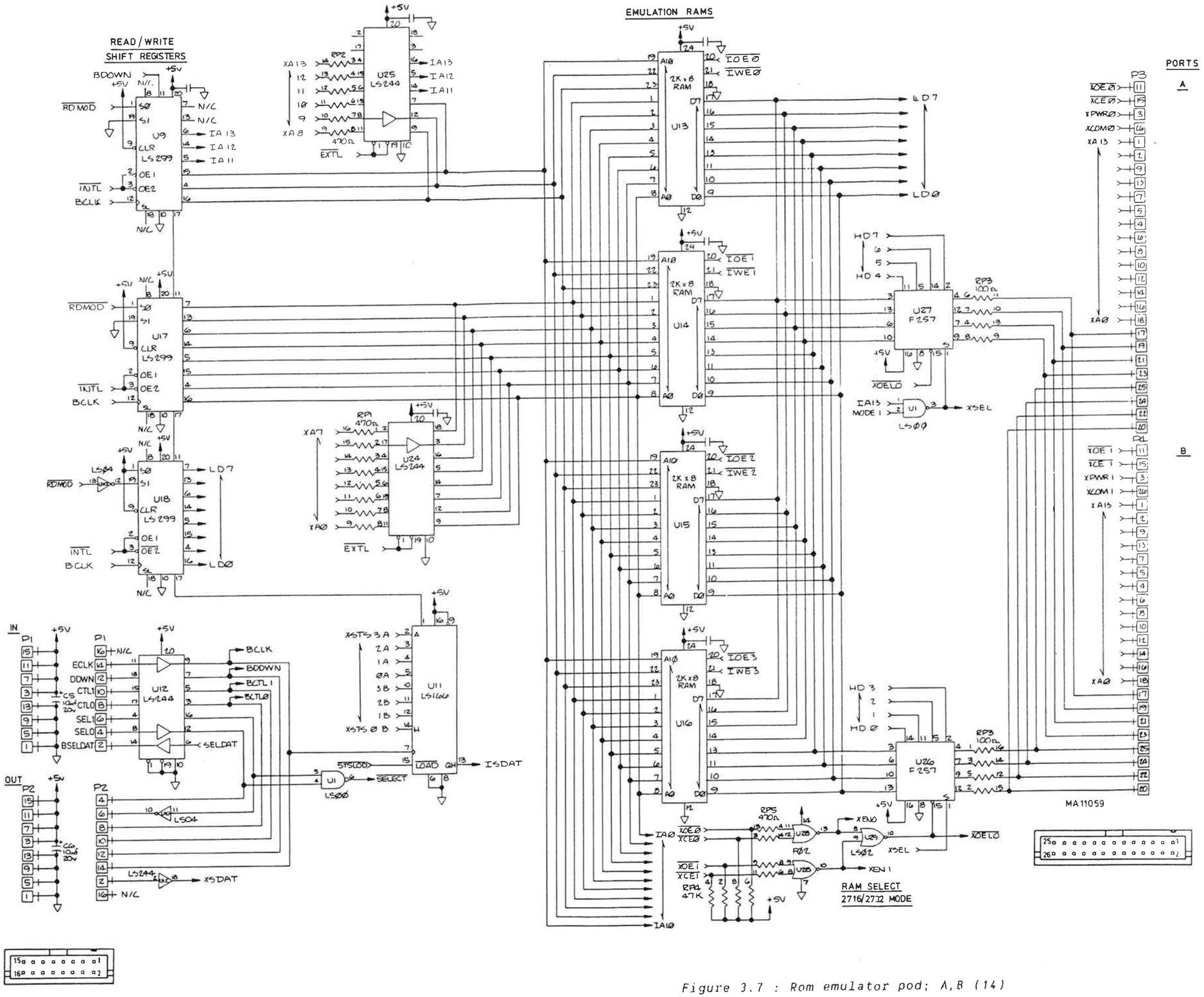
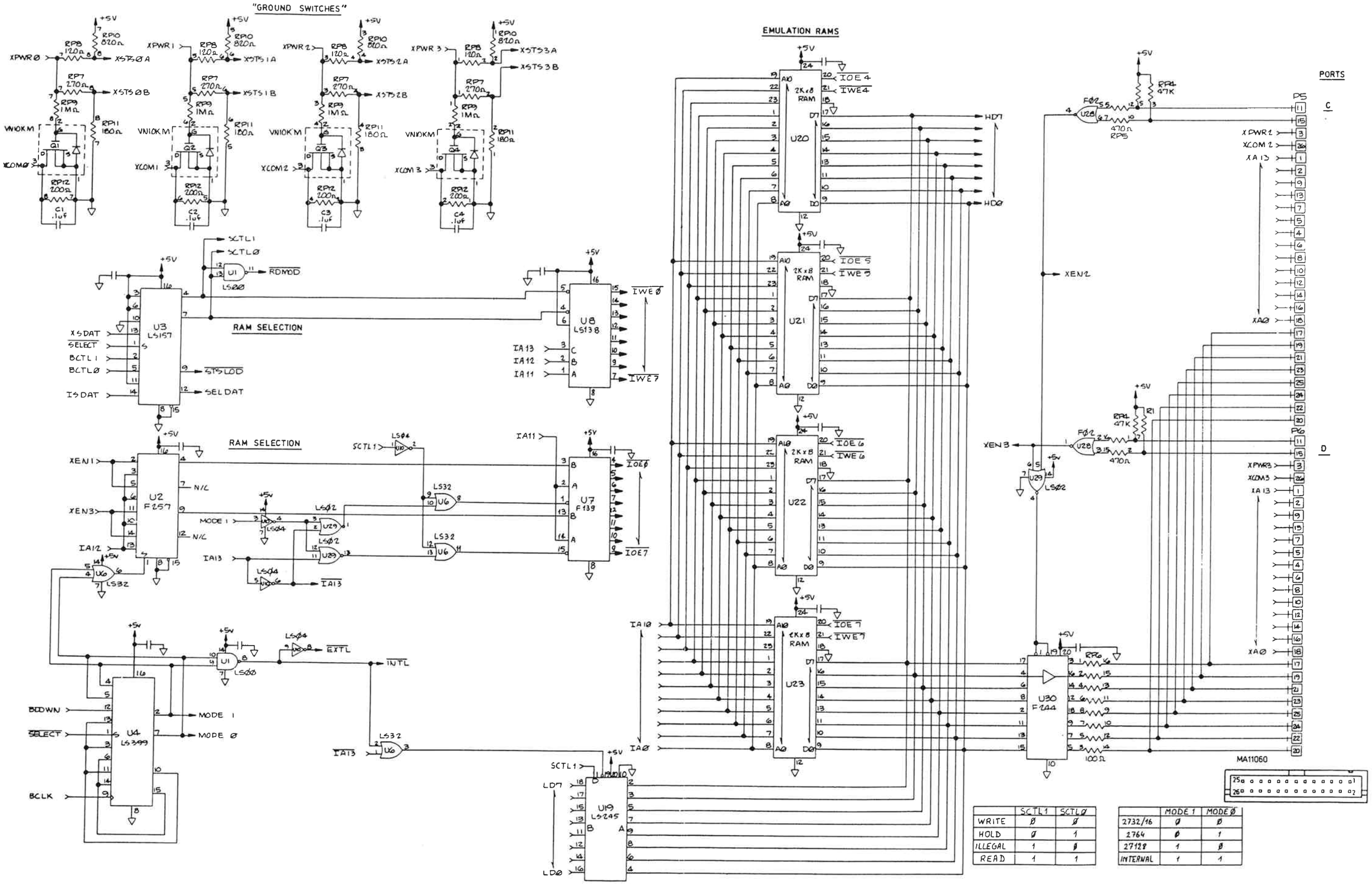


Figure 3.7 : Rom emulator pod; A,B (14)



	SCTL1	SCTL0
WRITE	0	0
HOLD	0	1
ILLEGAL	1	0
READ	1	1

	MODE 1	MODE 0
2732/16	0	0
2764	0	1
27128	1	0
INTERNAL	1	1

Figure 3.8 : Rom emulator pod: C,D (15)

LIST OF SIGNAL NAMES (diagram 15)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
BCLK	Buffered Rom emulator clock	14	15
BCTL0	Buffered control line 0	14	15
BCTL1	Buffered control line 1	14	15
BDOWN	Buffered data down	14	15
EXTL*	Select external (emulation) mode	15	14
HD0	Rom emulator data 0	15	14 BD
HD1	Rom emulator data 1	15	14 BD
HD2	Rom emulator data 2	15	14 BD
HD3	Rom emulator data 3	15	14 BD
HD4	Rom emulator data 4	15	14 BD
HD5	Rom emulator data 5	15	14 BD
HD6	Rom emulator data 6	15	14 BD
HD7	Rom emulator data 7	15	14 BD
IA 0	Addressline 0 (internal source)	14	15
IA 1	Addressline 1 (internal source)	14	15
IA 2	Addressline 2 (internal source)	14	15
IA 3	Addressline 3 (internal source)	14	15
IA 4	Addressline 4 (internal source)	14	15
IA 5	Addressline 5 (internal source)	14	15
IA 6	Addressline 6 (internal source)	14	15
IA 7	Addressline 7 (internal source)	14	15
IA 8	Addressline 8 (internal source)	14	15
IA 9	Addressline 9 (internal source)	14	15
IA10	Addressline 10 (internal source)	14	15
IA11	Addressline 11 (internal source)	14	15 ?
IA12	Addressline 12 (internal source)	14	15 ?
IA13	Addressline 13 (internal source)	14	15 ?
IA13*	Addressline 13 (internal source)	15	15
INTL*	Select internal mode	15	15
IOE0*	Output enable, (internal) RAM 0	15	14
IOE1*	Output enable, (internal) RAM 1	15	14
IOE2*	Output enable, (internal) RAM 2	15	14
IOE3*	Output enable, (internal) RAM 3	15	14
IOE4*	Output enable, (internal) RAM 4	15	15
IOE5*	Output enable, (internal) RAM 5	15	15
IOE6*	Output enable, (internal) RAM 6	15	15
IOE7*	Output enable, (internal) RAM 7	15	15
ISDAT	(internal) Serial data up	14	15
IWE0*	Write enable, (internal) RAM 0	15	14
IWE1*	Write enable, (internal) RAM 1	15	14
IWE2*	Write enable, (internal) RAM 2	15	14
IWE3*	Write enable, (internal) RAM 3	15	14
IWE4*	Write enable, (internal) RAM 4	15	15
IWE5*	Write enable, (internal) RAM 5	15	15
IWE6*	Write enable, (internal) RAM 6	15	15
IWE7*	Write enable, (internal) RAM 7	15	15
LD0	Rom emulator data 0	14	15 BD
LD1	Rom emulator data 1	14	15 BD
LD2	Rom emulator data 2	14	15 BD
LD3	Rom emulator data 3	14	15 BD
LD4	Rom emulator data 4	14	15 BD
LD5	Rom emulator data 5	14	15 BD
LD6	Rom emulator data 6	14	15 BD
LD7	Rom emulator data 7	14	15 BD

LIST OF SIGNAL NAMES (diagram 15)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
MODE 0	mode 0 select	15	not used
MODE 1	mode 1 select	15	14,15
ROMOD*	Select read mode	15	14
SCTL0	Selected control line 0	15	not used
SCTL1	Selected control line 1	15	15
SELOAT	Serial data up (to mainframe)	15	14
SELECT*	Select line	14	15
STSL00*	Load connection test data	15	14
XA 1	Addressline 1 (external source)	15	14 ?
XA10	Addressline 10 (external source)	15	14 ?
XA11	Addressline 11 (external source)	15	14 ?
XA12	Addressline 12 (external source)	15	14 ?
XA13	Addressline 13 (external source)	15	14 ?
XA 2	Addressline 2 (external source)	15	14 ?
XA 3	Addressline 3 (external source)	15	14 ?
XA 4	Addressline 4 (external source)	15	14 ?
XA 5	Addressline 5 (external source)	15	14 ?
XA 6	Addressline 6 (external source)	15	14 ?
XA 7	Addressline 7 (external source)	15	14 ?
XA 8	Addressline 8 (external source)	15	14 ?
XA 9	Addressline 9 (external source)	15	14 ?
XCOM0	Ground on port A (ext. source)	14	15
XCOM1	Ground on port B (ext. source)	14	15
XCOM2	Ground on port C (ext. source)	15	15
XCOM3	Ground on port D (ext. source)	15	15
XEN1	Select RAM for port B (ext.source)	14	15
XEN2	Select RAM for port C (ext.source)	15	not used
XEN2	Select RAM for port C (ext.source)	15	not used
XEN3	Select RAM for port D (ext.source)	15	15
XEN3	Select RAM for port D (ext.source)	15	15
XPWR0	Power on port A (ext. source)	14	15
XPWR1	Power on port B (ext. source)	14	15
XPWR2	Power on port C (ext. source)	15	15
XPWR3	Power on port D (ext. source)	15	15
XSDAT	Serial data up (from second pod)	14	15
XSTS0A	Conection test, port A	15	14
XSTS0B	Conection test, port A	15	14
XSTS1A	Conection test, port B	15	14
XSTS1B	Conection test, port B	15	14
XSTS2A	Conection test, port C	15	14
XSTS2B	Conection test, port C	15	14
XSTS3A	Conection test, port D	15	14
XSTS3B	Conection test, port D	15	14

3.6.4 Z80 MICROPROCESSOR POD (see figure 3.14) PM 8869 .

This pod supports the ZILOG Z80 and Z80/A/B/C microprocessor.

Data signals (DATA0...DATA7) and address lines (ADR0...ADR15) are first high impedance-buffered (U3, U5, U9) and then transferred to the input demultiplexers in the mainframe (SIG0...SIG23).
The data signals are also latched (clock pulse DLTCH; data latch) to meet the setup & hold time requirements.

Data inputs 24...27 (SIG24...SIG27) are used to take-in 4 status signals of the Z80. These are necessary for correct disassembly of the microprocessor instructions.
Status signal IOREQ* is latched by means of U10, U17. This latch is cleared immediately after the next external clock pulse (CLTCH; clear latch).
Data inputs 28...31 can be used to take-in user defined signals (via P3).

The microprocessor in the mainframe can read the identity of the pod by reading the contents of buffer U12. This is done via data lines 24...31.
When doing this, buffer U19 is disabled.

The selection between internal clock (BFCLKOUT) and external clock (EXTCLK) is done via U16 by means of signals BFPODSEL0 (buffered pod select), which comes from buffer U50 in the mainframe (see figure 2.7).
The selected clock (SCLK) goes up to the mainframe to clock the input demultiplexers.
Signals BFPODSEL0...BFPODSEL2 are also used to generate the control signals for reading buffer U12.
Signal MODE2 is used to disable the refresh clock (DRFSH;U10) in normal mode in order not to show the refresh cycles on the display.

The external clock signals are first compared to a fixed threshold voltage (U7, U11) and then wired-ored to generate the external clock (EXTCLK).
In internal mode (signal INT*; comes from BFPODSEL 1) the generation of clocks for the data latch and IOREQ* latch are stopped.
Signal MODE 2 stops the generation of the refresh clock signal (DRFSH) when the pod is in the normal mode and enables the clock in Z80REF mode.

To protect the pod against pod connection errors, ground of the system under test (X29) is only then connected to ground of the mainframe (via FET Q1) when the supply voltage (X11 of the microprocessor) is at the correct position at the microprocessor clip.
This is detected via U18-pin 12 and comparator U18-pin 10 (CONEXERR*).
The microprocessor in the mainframe reads this information via buffer U12 and will display POD CONNECTION ERROR if the pod is not connected properly.

LIST OF SIGNAL NAMES (diagram 20)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name. A ? indicates that the source cannot be defined (for example one signal-name can come from different pods, but only one can be connected). A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
AX11	Pin 11 of uP clip	20	20
AX20	Pin 20 of uP clip	20	20
AX21	Pin 21 of uP clip	20	20
AX22	Pin 22 of uP clip	20	20
AX29	Pin 29 of uP clip	20	20
BFPODSEL0	Buffered pod select 0	3	20
BFPODSEL1	Buffered pod select 1	3	20
BFPODSEL2	Buffered pod select 2	3	20
BFPODWRT*	Buffered pod write	3	20
CLTCH	Clear latch	20	20
CONEXERR*	Connection error	20	20
DLTCH	Clock for data latch	20	20
DRFSH	Refresh cycle	20	20
EXTCLK	External clock	20	20
INT*	Set to internal clock mode	20	20
IORQ*/AX20	Input/output request	20	20
M1*/AX27	Machine cycle 1	20	20
MODE 2	Set to Z80REF mode	20	20
MREQ	Memory request	20	20
QUALIN	Qualifier in signal	20	1,5
RD*/AX21	Read signal	20	20
READEN	Disable data buffer for id read	20	20
READEN*	Enable buffer for id read	20	20
SCLK	Selected clock	20	1,5
SIG 0	Input channel 0	20	1,5
SIG 1	Input channel 1	20	1,5
SIG 2	Input channel 2	20	1,5
SIG 3	Input channel 3	20	1,5
SIG 5	Input channel 5	20	1,5
SIG 6	Input channel 6	20	1,5
SIG 7	Input channel 7	20	1,5
SIG 8	Input channel 8	20	1,5
SIG 9	Input channel 9	20	1,5
SIG10	Input channel 10	20	1,5
SIG11	Input channel 11	20	1,5
SIG12	Input channel 12	20	1,5
SIG13	Input channel 13	20	1,5
SIG14	Input channel 14	20	1,5
SIG15	Input channel 15	20	1,5
SIG16	Input channel 16	20	1,5
SIG17	Input channel 17	20	1,5
SIG18	Input channel 20	20	1,5
SIG19	Input channel 20	20	1,5
SIG20	Input channel 20	20	1,5
SIG21	Input channel 21	20	1,5
SIG22	Input channel 22	20	1,5
SIG23	Input channel 23	20	1,5
SIG24	Input channel 24	20	1,3,5 BD
SIG25	Input channel 25	20	1,3,5 BD
SIG26	Input channel 26	20	1,3,5 BD
SIG27	Input channel 27	20	1,3,5 BD
SIG28	Input channel 28	20	1,3,5 BD
SIG29	Input channel 29	20	1,3,5 BD
SIG30	Input channel 30	20	1,3,5 BD
SIG31	Input channel 31	20	1,3,5 BD
WR*/AX22	Write signal	20	20

MODIFICATIONS:

In some applications, the target system will not work correct anymore after connection a PM 8869 microprocessor pod to it.
This can be caused by one of the following problems:

a. The "high" voltage of the target system is limited to +3Vdc by the 74hc ... input circuits inside the pod.
b. If a to high voltage apppear on the inputs of the comparators U7 and U11, coming from the target, U7 and U11 can be damaged.

Therefore the following modification have to be done in the PM 8869 pod.
All input circuits of the pod have to be changed into 74HCT ... in order to raise the "high" voltage of the target.
Place clamping diodes to the comparators to protect the inputs.
These modifications only have to be done when you have a "revision A" board in the pod (this revision has no revision indication, at the outside of the pod).
Proceed as follows:

A. Install HCT 240 for U15.
   Install HCT 244 for U3, U5, U9 and U14.
   Install HCT 00 for U17.
B. Cut trace (solder side) at RP5-pin 1, RP6-pin 1, RP7-pin 1
   Cut trace (component side) at RP8-pin 1.
   Cut trace (component side) near R17 and connector (GND trace).
   Cut trace (component side) between U5-pin 20 and bypass capacitor.
   Cut trace (solder side) near U3-pin 20.
C. Connect RP8-pin 1 to RP7-pin 1 then to connector P1-pin 20.
   Connect U5-pin 20 to capacitor C1 to the +pin.
   Connect U3-pin 20 to U2-pin 20.
   Connect U12-pin 2 to GND plane at connector P2.
   Connect U4-pin 1 to GND plane at connector P2.
   Connect 0.1 uF capacitor side of RP5-pin 1 cut to U3-pin 1.
D. Connect anodes of 1N914 diodes (4 places) to U7-pin 1, U7-pin12, U11-pin 1 and U11-pin 12.
   Connect all cathodes to capacitor C2 +pin.
E. Engrave the character "B" behind the serial number, at the back of the pod>

After these modifications, the pod has board revision B (indiacted by a character B engraved behind the serial number, at the outside of the pod).

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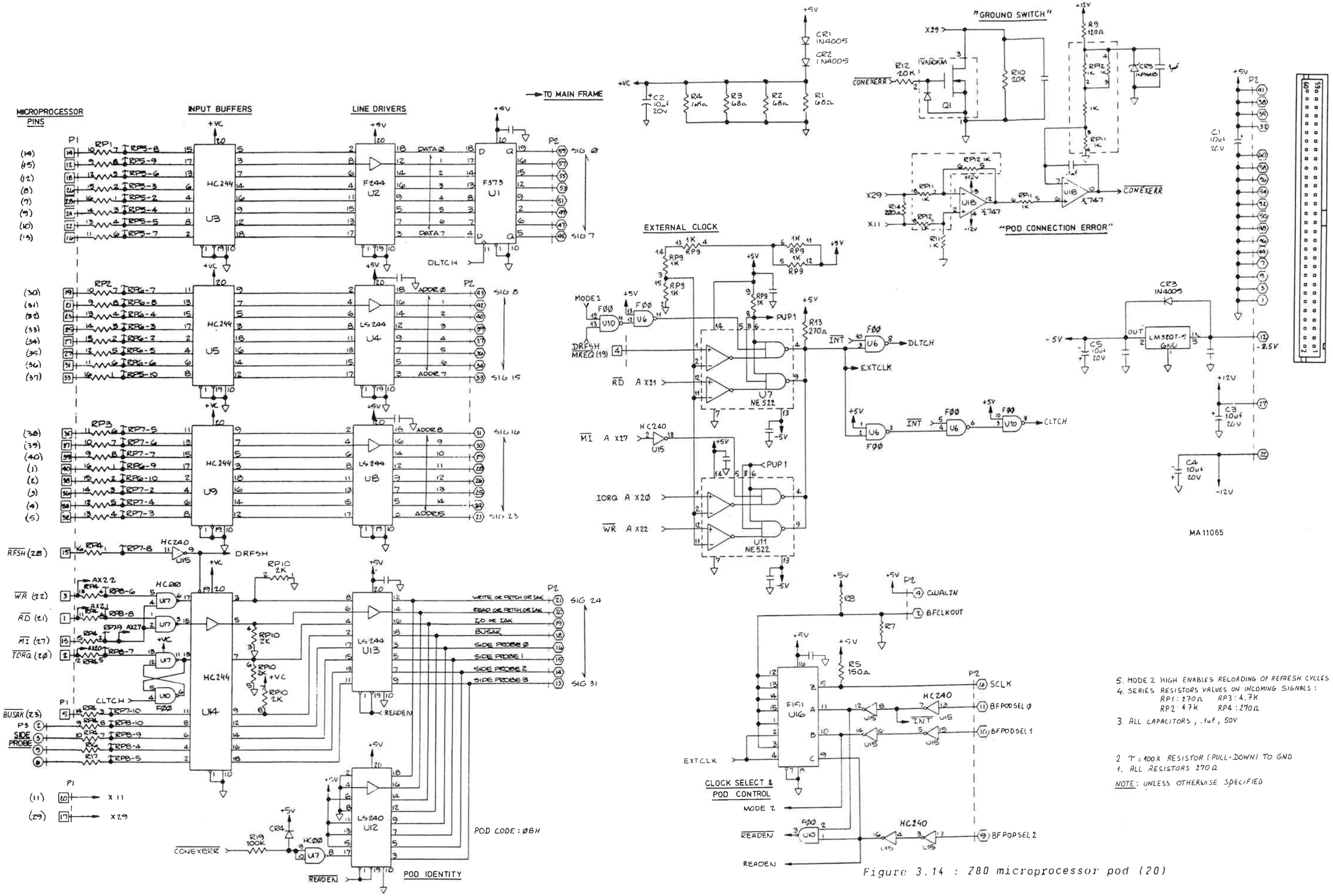


5. MODE 2 HIGH ENABLES RECORDING OF REFRESH CYCLES
4. SERIES RESISTORS VALUES ON INCOMING SIGNALS :
   RP1 : 270Ω RP3 : 4.7K
   RP2 : 4.7K RP4 : 270Ω
3. ALL CAPACITORS , .1uf , 50V

2. ↑ = 100K RESISTOR (PULL-DOWN) TO GND
1. ALL RESISTORS 270Ω

NOTE : UNLESS OTHERWISE SPECIFIED

Figure 3.14 : Z80 microprocessor pod (20)

3.6.5. NSC800 MICROPROCESSOR POD (see figure 3.15) PM 8870

This pod supports the NATIONAL SEMICONDUCTOR NSC800 microprocessor.

The multiplexed address and data bus is buffered in input bufferers U1 and U2. The data signals are again buffered by U15, and then latched into U16 (signal DLTCH, comes from clock generation) , before they are passed to the mainframe (SIG0 ... SIG7).
The address signals are clocked into output latch U3 on the ALE pulse, that comes from the microprocessor via U4. The outputs of U3 connect these address lines to the mainframe (SIG8 ... SIG15).
Address lines A8 ... A15 are also buffered first, and then latched before they are sent to the mainframe (SIG16 ... SIG23).

Status information from the microprocessor is passed to the mainframe via the upper half of buffer U7 and U8 (SIG24...SIG27).

Three spare lines are available for user-defined connections to the system under test. These signals are buffered via the lower half of U7 before they are transferred to the mainframe (SIG29 ... SIG31).

The selection between internal clock (BFCLKOUT) or external clock is done under control of the microprocessor by means of signals BFPODSEL0...BFPODSEL2 (buffered pod select) which come from buffer U50 in the mainframe (see figure 2.7).
As an external clock the RD*, WR*, and INTA* lines are used (signal MODE1*).
In the NSC800 REFESH mode, also the RFSHB (refresh signal) is used as a clock signal. In this mode, also refresh cycles will be recorded in the PM 3632 mainframe (signal MODE2*).
All clock signals are combined via NAND gates (12, U17), which means that when one of them goes low, a clock pulse will be generated for the mainframe.

The microprocessor in the mainframe can read the identity of the pod by reading the contents of the lower halfs of buffers U8 and U9. This is done via signal lines SIG24 ... SIG31.
When doing this, the higher halfs of these buffers are disabled (signal MODE4*).

To protect the pod against pod connection errors, ground of the system under test is only connected to ground of the mainframe (via FET Q1) when the supply voltage (40) is at the correct position of the microprocessor clip.
The microprocessor in the mainframe reads this information via buffer U9 and will display POD CONNECTION ERROR if the pod is not connected properly.

WARNING: When using the side probe, do not connect the ground wires! This will cause a short circuit between the drain and source of FET Q1.

3.8 PARTS LIST, PODS.

This list contains all components which are not standard.

The p.c. boards for the pods are not available from concern service. When, however, you need a spare p.c. board for a particular pod, you have to order it via the commercial department.

POSITION NUMBER	DESCRIPTION	ORDERING CODE
STANDARD LOGIC POD PM 8860		
Integrated circuits:		
U18	74LS244	5322 209 86017
U13	74LS132	5322 209 85201
U21	74LS175	5322 209 84999
U26,25	74F194	5322 209 82418
U22	74LS240	5322 209 85862
U29,33	74F244	5322 209 81128
U9,14,26	74F374	5322 209 81909
U30	uA747	5322 209 84781
U10,11,15-17	NE521	5322 209 14441
U19,20,23,24	NE521	5322 209 14441
U27,28,31,32	NE521	5322 209 14441
U3,4,7,8,12	NE521	5322 209 86462
VR1	LM320T-5	5322 209 82842
Semi conductors:		
CR3,7	1N914B	5322 209 31487
CR5,6	1N961B	5322 209 34786
Various:		
CA	CAP-6.8PF,NP0,500V	5322 122 32275
CB	CAP-27PF,NP0,500V	5322 122 32274
P1A	CONNECTOR 26 PIN	5322 265 51111
P1B	CONNECTOR 20 PIN	5322 265 51109
P2	CONNECTOR 60 PIN	5322 265 61059
RA	RES. NETW. 82K 8 PINS	5322 111 90841
RA	RES. NETW. 82K 6 PINS	5322 111 90839
RB	RES. NETW. 18K 10 PINS	5322 111 90837
RB	RES. NETW. 18K 6 PINS	5322 111 90838
RC	RES. NETW. 1K	5322 111 94144
RD	RES. NETW. 2K2	5322 111 90469
RF	RES. NETW. 330E	5322 111 90295
S1	SLIDE SWITCH	5322 277 10848

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

4 CHANNEL FAST POD PM 8862

Integrated circuits:

U5	74LS 37	4822 209 80916
U1	74LS132	5322 209 85201
U4	74LS175	5322 209 84999
U3	74LS240	5322 209 85862
U15	74F244	5322 209 81128
U2,6	SG3524	5322 209 81508
U9,20	F100102	5322 209 82875
U7	F100124	5322 209 82876
U16	F100125	5322 209 82877
U8,19	F100131	5322 209 82878
U17,18	F100151	5322 209 82879
U11,24	LM55CN	5322 209 85824
U13	LM1458N	5322 209 84488
U10,12,14	AD9685BH	5322 209 82841
U21,22,23	AD9685BH	5322 209 82841

Semi conductors:

Q4	T1P31A	5322 130 42504
Q2	T1P32A	5322 130 44333
Q1	2N2222A	5322 130 44115
Q3	2N2907A	5322 130 40621
CR5	1N5400	5322 130 31624
CR3,CR4	1N5820	5322 130 54064
CR7	1N756A	5322 130 32215
CR6	1N757A	5322 130 30682
CR9	1N914B	5322 130 31487
CR8	1N753A	4822 130 34167
CR1,CR2	1N4005	5322 130 34323
CR10,CR11	1N749A	5322 130 31837
CR12,CR13	1N750A	5322 130 34555

Various:

L1	COIL	5322 158 10743
L2	COIL	5322 158 10744
DL1,2,5,6	DELAY LINE 6 nsec	5322 320 40128
DL3,4,7,8	DELAY LINE 2 nsec	5322 320 40127
K1,K2	RELAY	5322 280 80552
R15,R23	RESISTOR 0.1E 1W	5322 113 31017
RL1-RL5	RES.NETW. 47E	5322 111 90846
RA	RES.NETW. 18K	5322 111 90854
RB	RES.NETW. 33K	5322 111 94071
RC	RES.NETW. 1K	5322 111 94176
RJ,RK	RES.NETW. 100E	5322 111 90786
RH	RES.NETW. 100E	5322 111 90787
R32	POTENTIOMETER 10K	5322 103 10269
S1	SLIDE SWITCH	5322 277 10848
J1	CONNECTOR 60 PIN	5322 265 61059

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

ROM EMULATOR POD PM 8864

Integrated circuits:

U1	74LS00	5322 209 84823
U29	74LS02	5322 209 85407
U2P	74F02	5322 209 81535
U10	74F04	4822 209 80783
U6	74LS32	5322 209 85311
U7	74F139	5322 209 82234
U3	74LS157	5322 209 81521
U11	74LS166	5322 209 86292
U12,24,23	74LS244	5322 209 86017
U30	74F244	5322 209 81128
U19	74LS245	5322 209 86225
U26,27	74F257	5322 209 81767
U2	74LS257	5322 209 86392
U9,17,18	74LS299	5322 209 86002
U13,16	M58725P	5322 209 82855
U20-23	M58725P	5322 209 82855
U4	74LS399	5322 209 82863

Semiconductors:

Q1-Q4	VN10KM	5322 130 42516

Various:

P1,2	CONNECTOR 16 PIN	5322 265 40461
P3-P6	CONNECTOR 26 PIN	5322 265 51111
RP3,6	RES. NETW. 100E	5322 111 90851
RP1,2 5	RES. NETW. 470E	5322 111 94054
RP8	RES. NETW. 120E	5322 111 90849
RP11	RES. NETW. 180E	5322 111 90844
RP7	RES. NETW. 270E	5322 111 94157
RP10	RES. NETW. 820E	5322 111 90847
RP4	RES. NETW. 47K	5322 111 90853
RP9	RES. NETW. 220K	5322 111 90845

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

STANDARD BUS POD PM 8863

Integrated circuits:

1C	74LS10	5322 209 84996
IE	74LS132	5322 209 85201
2B,2C,3C,3D	74LS244	5322 209 86017
2D	74LS374	5322 209 85869
1A,1D	74F00	5322 209 81534
2A	74F151	5322 209 81678
3E	74F244	5322 209 81128
2E	74F373	5322 209 81533
1B	74HC00	4822 209 82377
3A,4A,4C	74HC244	5322 209 82861
3B,4B	74HC257	5322 209 82862
5C,5D	NE522	5322 209 86462
VR 1	LM320T-5	5322 209 82842

Semiconductors:

CR6	1N914B	5322 130 31487
CR1-CR5,CR7	1N4005	5322 130 34323
Q1	VN10KM	5322 130 42516

Various:

RP1-RP5	RES. NETW. 100K	5322 111 94202
RA,B,F,6A	RES. NETW. 270E	5322 111 90852
5E,6B,6C	RES. NETW. 1K	5322 111 90848
P2	CONNECTOR 60 PIN	5322 267 70161

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

8085, 8048, (FAMILY), 8051 (FAMILY) MICROPROCESSOR POD PM 8865

Integrated circuits:

U3	74F00	5322 209 81534
U9	74HCT10P	5322 209 11107
U2	74F32	5322 209 82133
U8	74LS139	5322 209 14876
U7	74F151	5322 209 81678
U12	74F240	5322 209 81127
U1,4,6,18,19	74LS244	5322 209 86017
U15,20	74HCT244P	5322 209 11116
U5,10,16,17	74HCT257P	5322 209 11114
U4	74LS279	5322 209 85346
U11	74F374	5322 209 81909
U13	74LS374	5322 209 85869

Semiconductors:

CR1,2	1N914B	5322 130 31487
Q1	VN10KM	5322 130 42516

Various:

K1,K2	RELAY	5322 280 70267
RP2,4,5,7	RES. NETW. 270E	5322 111 90871
RP1,3,6,8	RES. NETW. 100K	5322 111 94227
RP9	RES. NETW. 3.3K	5322 111 90872
S1	4 POS. DIP SWITCH	5322 276 40351
P1	CONNECTOR 40 PIN	5322 267 70159
P2	CONNECTOR 60 PIN	5322 267 70161
P3	CONNECTOR 20 PIN	5322 267 51109
-	POD PC BOARD ONLY	5322 216 21769
-	TEST CLIP 40-PIN FOR MODIFICATION	5322 321 22551

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

MICROPROCESSOR PODS PM 8866, PM 8867, PM 8868

PM 8866 :6800, 6802, 6808
PM 8867 :6809, 6809E
PM 8868 :6502, 6512, 65C02, 65C102, 65C112

Integrated circuits:

U2	74HC257	5322 209 82862
U1,9,13,16	74HCT244	5322 209 11116
U4	74HCT00	
U8	74F151	5322 209 81678
U12	74F00	5322 209 81534
U3	74F373	5322 209 81533
U7,11	NE522	5322 209 86462
U6,10,14,17	74LS244	5322 209 86017
U5	uA747	5322 209 84781
VR1	LM320T-5	5322 209 82842

Semiconductors:

CR1,2,6,7,8,9	1N914B	5322 130 31487
CR3	1N961B	5322 130 34786
CR4,5	1N4005	5322 130 34323
Q1	VN10KM	5322 130 42516

Various:

S1	4 POS. DIP SWITCH	5322 276 40352
RN1,2	RES. NETW. 1K	5322 111 90848
RN3,4,5	RES. NETW. 4.7K	5322 111 90873
RN6	RES. NETW. 1K	5322 111 90848
K1	RELAY	5322 280 70267
-	PC BOARD PM 8866	5322 216 21771
-	PC BOARD PM 8867	5322 216 21772
-	PC BOARD PM 8868	5322 216 21735
P 1	CONNECTOR 40 PIN	5322 267 70161
P 2	CONNECTOR 60 PIN	5322 267 70159
P 3	CONNECTOR 20 PIN	5322 267 51109

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

Z80 MICROPROCESSOR POD PM 8869

Integrated circuits:

U15	74HCT240	
U6,10	74F00	5322 209 81534
U17	74HCT00	
U16	74F151	5322 209 81678
U2	74F244	5322 209 81128
U4,8,13	74LS244	5322 209 86017
U3,5,9,14	74HCT244	5322 209 11116
U1	74F373	5322 209 81533
U7,11	NE522	5322 209 86462
U12	74LS240	5322 209 85862
U18	uA747	5322 209 84781
VR1	LM320LZ-5	5322 209 82884

Semiconductors:

CR3,4,6,7,8,9	1N914B	5322 130 31487
CR1,2	1N4005	5322 130 34323
Q1	VN10KM	5322 130 42516
CR5	1N961B	5322 130 34786

Various:

RP9	RES. NETW. 1K	5322 111 90848
RP1,4	RES. NETW. 270E	5322 111 90852
RP5,6,7,8	RES. NETW. 100K	5322 111 94202
RP2,3	RES. NETW. 4.7K	5322 111 90873
RP11,12	RES. NETW. 1K	5322 111 94152
RP10	RES. NETW. 2K	5322 111 90468
P1	CONNECTOR 40 PIN	5322 267 70159
P2	CONNECTOR 60 PIN	5322 267 70161
P3	CONNECTOR 20 PIN	5322 267 51109
-	PC BOARD POD	5322 216 21734

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

NSC800 MICROPROCESSOR POD PM 8870

Integrated circuits:

U1,2,5,7	74HC244	5322 209 82861
U15	74LS244	5322 209 86017
U3,6	74LS374	5322 209 85869
U8,9	74LS257	5322 209 86392
U16	74F373	5322 209 81533
U12	74HC20	5322 209 83206
U13	74LS74	5322 209 80782
U4	74HC00	5322 209 82377
U10	74LS32	5322 209 85311
U17	74F02	5322 209 81535
U14	74F151	5322 209 81678
U11	74LS04	4822 209 80783

Semiconductors:

Q1	MOSFET VN10KM	5322 130 42516
CR3,4	DIODE 1N914	5322 130 31487
CR5	DIODE 1N753A	5322 130 34167
CR1,2	DIODE 1N4005	5322 130 30799

Various:

P 1	CONNECTOR 40 PIN	5322 267 70159
P 2	CONNECTOR 60 PIN	5322 267 70161
P 3	CONNECTOR 20 PIN	5322 267 51109
-	PC BOARD POD	5322 216 21773

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

68000/68010 MICROPROCESSOR POD PM 8874

Integrated circuits:

UD2-UD5,UE2-UE4	74ALS374	5322 209 81646
UF8,UF9,UG1,UG2,UG6	74ALS374	5322 209 81646
UC1,UH1,UH7	74ALS374	5322 209 81646
UH5	74ALS273	5322 209 85792
UG7,UF6,UF7,UJ4,UJ5,UH4	74HC257	5322 209 82862
UH6,UG5	74HC257	5322 209 82862
UF10	SG3524	5322 209 81508
UF5,UG4,UH3	74F283	5322 209 81588
UF4,UJ2	74F521	5322 209 81543
UI1,UK5,UK7,UJ9	74F74	5322 209 81474
UK2	74F00	5322 209 81534
UJ1	74F04	5322 209 81577
UK10	74F174	5322 209 83326
UK1,UK6,UH8	74F32	5322 209 82133
UC6	LM1458N	5322 209 84488
UG9,UH9	74F399	5322 209 82852
UH2	74F374	5322 209 81909
UL10,UG3	74LS244	5322 209 86017
UJ8	74F08	5322 209 81574
UK3,UL1	74F10	5322 209 81681
UJ3	74F283	5322 209 81588
UG8	74F161	5322 209 82001
UA2	74ALS257	5322 209 81638
UK4	150 nsec DELAY LINE	5322 320 40129

Semiconductors:

CR2	1N5822	5322 130 32677
CR1,4	1N914	5322 130 31487
CR3	TRANSORB. 5V 1.5KW	5322 130 34762
Q1	2N2907A	5322 130 40621
Q2	TIP120	5322 130 44529
Q3	VN10KM	5322 130 42516

Various:

-	PC BOARD POD	5322 216 21717
-	60 POLE FLAT CABLE + 60 POLE CLIP	5322 321 21322
UE9-UF9	PROM DC68KP PROG.	5322 209 50579
UG9-UH9	PROM ST68 PROG.	5322 209 50581

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

8086/8088 MICROPROCESSOR POD PM 8876

Integrated circuits:

U1	74F244	5322 209 81128
U2,4,6,7	74HCT374	5322 209 11119
U3,5	74S374	5322 209 86162
U8,10	74F164	5322 209 82371
U9,25	74ALS374	5322 209 81646
U11,12,13,14,15,16	74F189	5322 209 83449
U17,18,19,20,21,22	74F189	5322 209 83449
U26,27,34	74F189	5322 209 83449
U23,24,28,29,30,31	74AL373	5322 209 83446
U32,33	74AL373	5322 209 83446
U38	74F174	5322 209 83326
U39,40,63	74AL253	5322 209 83444
U41	74F158	5322 209 81532
U45,46	74172	5322 209 83448
U47	74ALS74	5322 209 83447
U48,52,64	74F74	5322 209 81474
U49	74ALS00	5322 209 83442
U50,54	74F64	5322 209 81538
U51	74F10	5322 209 81681
U53,57	74F08	5322 209 81574
U55,59	74F157	5322 209 81531
U56	74F86	5322 209 81539
U58	74ALS32	5322 209 83445
U60	SG3524	5322 209 82843
U61	74LS399	5322 209 82863
U62	74F02	5322 209 81535
U66	74F04	5322 209 81577
U68	DELAY LINE 50 nsec	5322 209 82417
U65	74ALS02	5322 209 83443

Semiconductors:

CR1	DIODE 1N914B	5322 130 31487
CR2	DIODE 1N5822	5322 130 32677
CR3	DIODE ICTE-5	5322 130 34762
Q1	2N2907	5322 130 40218
Q2	TIP140	5322 130 42763
Q3,4	VN10KM	5322 130 42516

Various:

-	PC BOARD POD	5322 216 21718
-	40 POLE FLAT CABLE + 40 POLE CLIP	5322 321 21323
U42	PROM 86ROM S.W REV. A	5322 209 50578

Pals are till further notice only available from Supply Centre Service group in Eindhoven.
Address: NEDERLANDSE PHILIPS BEDRIJVEN B.V.
I & E DIVISION
SERVICE T&M DTS
BUILDING TQ V-2
Att. Mr. F. Wienia

DESCRIPTION			VALUE	QUANTITY	ORDERING NUMBER
SERIAL DATA POD PM 8811/20					
Integrated circuits:					
INT. CIRCUIT	HEF4049BD			5	4822 209 10306
INT. CIRCUIT	HEF4029BD			4	4822 209 10302
INT. CIRCUIT	HEF4071BD			2	4822 209 10307
INT. CIRCUIT	HEF4073BD			2	4822 209 10266
INT. CIRCUIT	HEF4013BD			2	4822 209 10248
INT. CIRCUIT	HEF40106BD			1	4822 209 10318
INT. CIRCUIT	74F109PC			1	5322 209 81669
INT. CIRCUIT	74F74PC			2	5322 209 81474
INT. CIRCUIT	74F02PC			1	5322 209 81535
INT. CIRCUIT	SN74LS157N-00			3	5322 209 81521
INT. CIRCUIT	HD1-6402C-9			2	5322 209 81661
INT. CIRCUIT	COM8146			1	5322 209 81671
INT. CIRCUIT	MC1489AN			2	5322 209 86511
Semiconductors:					
LF TRANSISTOR	BC549C			9	4822 130 44246
LF TRANSISTOR	BC559B			7	4822 130 44358
SIL. DIODE	BAX12 DO-35			3	5322 130 34605
LED RED	CQW24-II			5	5322 130 32085
Resistors:					
MTL. FILM RST.	MR25	1%	649E	5	5322 116 54532
MTL. FILM RST.	MR25	1%	100E	2	5322 116 55549
MTL. FILM RST.	MR25	1%	511E	2	4822 116 51282
MTL. FILM RST.	MR25	1%	825E	2	5322 116 54541
MTL. FILM RST.	MR25	1%	2K	6	5322 116 54572
MTL. FILM RST.	MR25	1%	5K11	1	5322 116 54595
MTL. FILM RST.	MR25	1%	10K	20	4822 116 51253
MTL. FILM RST.	MR25	1%	16K9	6	5322 116 54635
PTC THERM. DISC	50V	15E	40E	2	4822 116 40001
HIGH VOLT. RST.	VR25	5%	5M6	7	4822 110 72207

DESCRIPTION			VALUE	QUANTITY	ORDERING NUMBER
Capacitors:					
CER. CAP. 2	100V	10%	470pF	9	4822 122 30034
CER. CAP. 1B	100V	2%	100pF	1	4822 122 31316
CER. CAP. SPRAQUE	50V	10%	100nF	39	5322 122 30108
ELCAP.	16V	-10%+50%	150uF	4	5322 124 24138
Various:					
SWITCH 1-P				1	4822 276 11076
MINI CODE SWITCH 30V 50 mA				2	5322 273 30291
SLIDE SWITCH 4P 2POS. PW				1	5322 277 60208
SLIDE SWITCH				5	5322 277 24053
CON. RH BUS 15-P HKS				1	5322 290 60436
CON. RH PIN 15-P HKS				4	5322 290 60435
REK. PAN CON. HKS 25-P PIN DIPS				1	5322 265 54055
HF-CON. BNC BUS				2	5322 267 10004
CRYSTAL 5068.8 KHz				1	5322 242 70691
PUSH BUTTON				1	4822 410 22363
SWITCH KNOB				2	5322 414 30038
KNOB COVER				2	5322 414 70015
Flat cables:					
BK CON PIN 15-P D-CON				4	5322 265 64115
BK CON BUS 15-P D-CON				4	5322 265 40241
BK CON BUS 25-P D-CON				2	5322 267 60129
BK CON PIN 25-P D-CON				1	5322 264 61001
SPACER ST ZN M3x40				2	5322 532 11104
SCREW WR ST M3x8				4	5322 502 30268

POSITION NUMBER	DESCRIPTION	ORDERING NUMBER

SERIAL ADAPTER PM 8812

Integrated circuits

U 1	74LS132	5322 209 85201
U 2	74LS244N	5322 209 86017
U 3	74F373	5322 209 81533
U 4	74HCT244	5322 209 11116
U 5	74LS175	5322 209 84999
U 6	LM556	
U 7	74F32	5322 209 82133
U 8	74F153	5322 209 81575
U 9	74F240	5322 209 81127
U 10	74LS74	5322 209 85869
U 11,12	74F374	5322 209 81909
U 13	7407	5322 209 84761

Mechanical parts

Connector	Description	ordering number
J 1,2	60-pins edge	5322 267 70161
J 3	20-pins edge, right angle	5322 267 51109
SW1	switch, pushbutton, momentary, spdt	

4. OPTIONS, CIRCUIT DESCRIPTION

4.1 GENERAL

This chapter describes all the options which are available for the PM 3632 logic analyzer.

A block diagram for the options is not enclosed. Figure 1.2, however, shows how the option boards are connected to the PM 3632 microprocessor bus.

A separate description of the setup memory (PM 8880/40) is not enclosed, because this option is a part of the setup data memory (PM 8880/50) and will be described there.

NOTE:

The setup and the setup data memory options can not be used together in one mainframe.

The PM 3632 has three options slots which can contain any combination of option cards.

These circuit desciptions contain no unit drawings. All component numbers are printed on the p.c. board which makes them self-explanatory.

In all circuit descriptions, a * behind a signal name indicates that it is low active. In the diagrams, the corresponding signal name has a bar above it.

4.2 DISA ROM BOARD (see figure 4.1)

This option board is used for disassembly of the microprocessor instructions, and can be plugged-in at any of the eight available positions.
The disa ROM can be a 2732, 2764 or a 27128.

Connector P1 connects the ROM disa board to the address, data and control busses ofg the microprocessor on the capture board.
Data and address lines are first buffered (U15, U16) before they are applied to the disassembler PROMs (U1...U8). The lower address lines are also latched in U11 (by means of the ALE pulse). The data bus on the option board is disconnected from the microprocessor databus when the option board is not selected (signal OPSEL via U17).

The option board is selected via signal OPSEL which is one of the three option select lines (OPSEL0....OPSEL2) that come from the microprocessor (U15, see figure 2.7). Because the option board can be in any of the three slots, the select signal is just called OPSEL. At power-up, the uP first reads the identity of the option boards in the slots (by reading buffer U10) and then knows which of the three OPSEL0...OPSEL2 lines it has to active to access the disa Rom board.
At power-up it also reads which disassembler PROMs are installed, and in which socket they are.

Decoder U18 is enabled only when the option board is selected (signal OPSEL) and when address line A15 is high (addresses 8000 and up; see also memory map figure 2.5). This decoder selects either the scratch pad RAM (U9, signal RAMEN*), the 'identity buffer ' (U10) or the bankselect register (U13, signal SELREG*).
This bank select register (U13) decodes the databus to select one of the 8 disa PROMs (via U12). The microprocessor can read the selected PROM back via register U14 (used at power-up, for reading the position of the PROMs).

LIST OF SIGNAL NAMES (diagram 21)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	21
A 8	Addressline 8	2	21
A 9	Addressline 9	2	21
A10	Addressline 10	2	21
A11	Addressline 11	2	21
A12	Addressline 12	2	21
A13	Addressline 13	2	21
A14	Addressline 14	2	21
A15	Addressline 15	2	21
AD0	Address/data line 0	2	21
AD1	Address/data line 1	2	21
AD14*	Address/data line 14	21	21
AD15*	Address/data line 15	21	21
AD2	Address/data line 2	2	21
AD3	Address/data line 3	2	21
AD4	Address/data line 4	2	21
AD5	Address/data line 5	2	21
AD6	Address/data line 6	2	21
AD7	Address/data line 7	2	21
ALE	Address latch enable	2	21
BRD*	Buffered read signal	21	21
BRDSEL*	Board selection signal	21	21
BWR*	Buffered write signal	21	21
IO/M*	Input,output/ memory	2	21
OPINT*	Option interrupt	21	1,2,6
OPSEL*	Option select; slot 0,1 or 2	3	21
RAMEN*	Enable scratch pad ram	21	21
RD*	Read signal	2	21
READY	Ready	21	1,2,6
RESET OUT	Reset out signal	2	21
ROM0*	Select disa rom 0	21	21
ROM1*	Select disa rom 1	21	21
ROM2*	Select disa rom 2	21	21
ROM3*	Select disa rom 3	21	21
ROM4*	Select disa rom 4	21	21
ROM5*	Select disa rom 5	21	21
ROM6*	Select disa rom 6	21	21
ROM7*	Select disa rom 7	21	21
S0	Status line 0	2	21
S1	Status line 1	2	21
SELREG*	Select bank switch register	21	21
WR*	Write signal	2	21

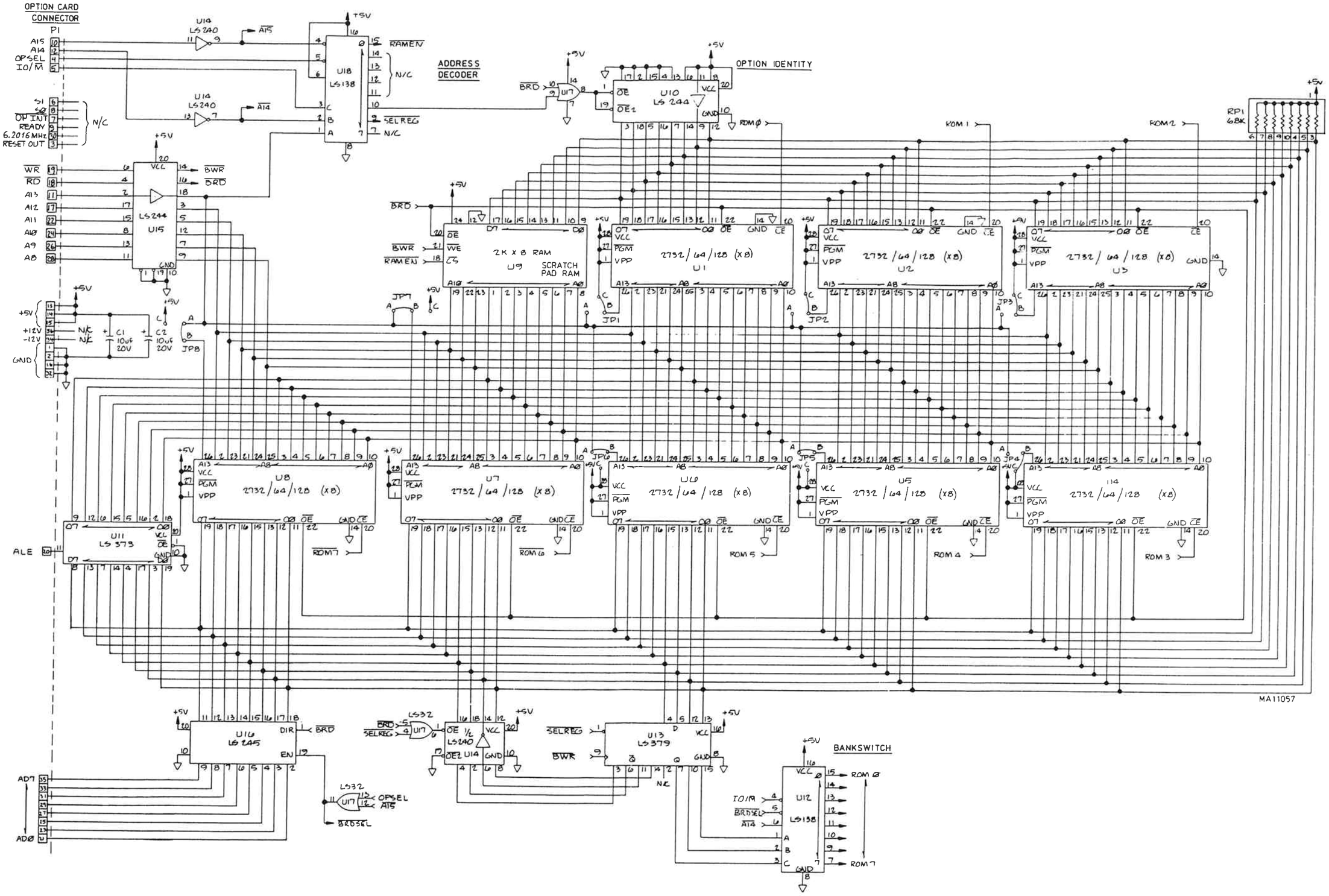


Figure 4.1 : Disa ROM board (21)

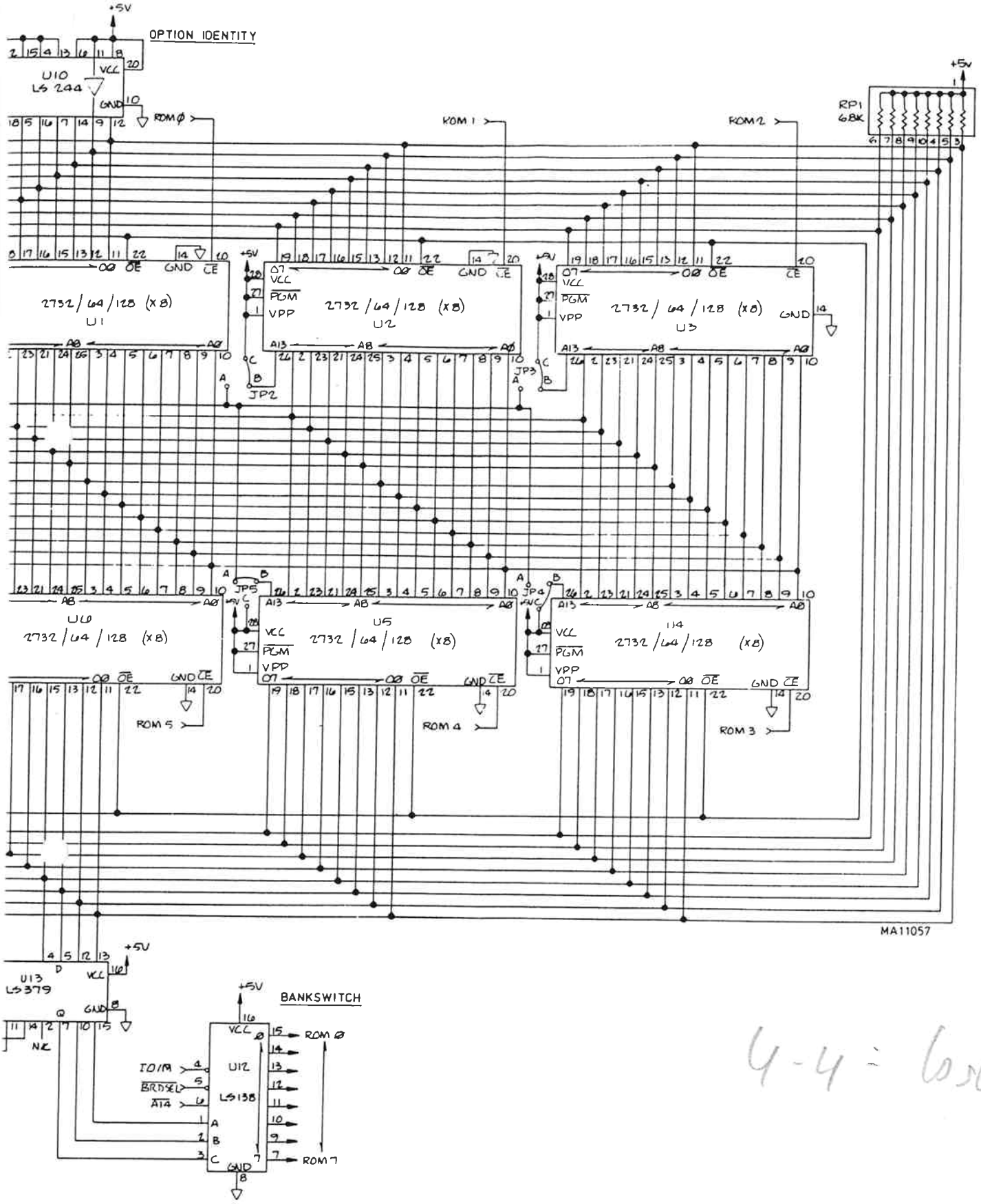


Figure 4.1 : Disa ROM board (21)

4-4 = lost...

4.3 RS 232C CONTROL CARD.

This option board is used for uploading or downloading of data (in data memory option, setup memory option or Rom emulator pod) to or from any device which can communicate via an RS 232C link (in hex format).
This board is also used to control the Rom emulator pod via another serial link (not an RS 232C link).
The option board can be plugged-in at any option slot at the capture board, but the most left slot is preferred (J3).

Connector P1 connects the RS 232C control card to the address, data and control busses of the microprocessor on the capture board.
Data lines are first buffered via U15 and are only connected to the microprocessor databus when this option board is selected (signal OPSEL, via U10). The lower address lines are latched in U11 (by meansof the ALE pulse). The upper address lines are directly applied to PROM U6.

The option board is selected via signal OPSEL which is one of the three option select lines (OPSEL0....OPSEL2) that come from the microprocessor (U15, see figure 2.7). Because the option board can be in any of the three slots, the select signal is just called OPSEL. The microprocessor first reads the identity of the option boards in the slots (by reading buffer U2) and then knows which of the three OPSEL0...OPSEL2 lines it has to activate to access RS 232C control card.

Decoder U5 is only enabled when the option board is selected (OPSEL), and when address line A15 is high (addresses 8000 and up; see also figure 2.5, memory map). This decoder either selects PROM U6 (via ROMEN*, memory mapped), scratch pod RAM U7 (via RAMEN*, memory mapped), UART U12 (via UARTEN*, I/O mapped) or the 'identity buffer' U2 (via TYPEN*,I/O mapped).

The control software for the RS 232 control card is located on the option board itself (U6). This software controls the RS 232C connection (via UART U12) and the serial link for the ROM emulator pod (via 8155 U7).

RS 232C control:
The RS 232C connection is only a three wire connection: TXD, RXD and DSR.
The RS 232C connection is controlled via UART U12 which is loaded with the correct control data by the microprocessor, before it starts receiving or transmitting data via RXD and TXD lines.
The UART interrupts the microprocessor when it needs to fill the transmitter buffer when it is empty (via signal TXEMPTY) or when the uP needs to empty the receiver buffer when it is full (via signal RXRDY).
These signals interrupt the microprocessor via the INT* input via U9, U10 and U14. The interrupt is enabled by the micrprocessor only when it has activated this board (signal INTEN* via 8155 U7).
The interrupt for the transmitter buffer is only enabled when the RS 232C control card is in transmitter mode (signal TXIDIS*; loaded by software in control register of UART).
The clock for the UART is derived from the microprocessor clock (6.2016 MHz for instruments connected to a 50 Hz mains) via clock divider U1 (approx. 3.2 MHz). The baudrate clock is derived via the timer portion of U7 (freq.= 16 times the selected baudrate). This timer is loaded immediately after starting data transfer.

Modification on the RS232-C control card

When there are problems with transferring data from the rom emulator pod, via the RS232-C control card to another device (for example a prom programmer), the following modifications have to be done.
Without modification,the prom programmer will give an incorrect chechsum after data is transferred from rom emulator pod to the prom programmer. Also in this case, calculating a checksum of the rom emulator pod contents by the PM 3632 itself will give incorrect results.
A new circuit diagram is enclosed .

Proceed as follows:

- Add one IC (47F175 = 5322 209 81542) on the RS232-C control card. This chip fits in the SPARE position next to U9.
- Cut the trace that leads from U7-pin 22 to U4-pin 9 (component side).
- Cut the trace that leads from U7-pin 24 to U4-pin 1 (component side).
- Add a wire between "74F175"-pin 1 and "74F175"-pin 16.
- Add a wire between "74F175"-pin 12 and "74F175"-pin 13.
- Add a wire between "74F175"-pin 16 and "74F175"-pin 13.
- Add a wire between "74F157"-pin 16 and U9-pin 14.
- Add a wire between "74F157"-pin 8 and U9-pin 7.
- Add a wire between "74F157"-pin 2 and U4-pin 1.
- Add a wire between "74F157"-pin 4 and U7-pin 24.
- Add a wire between "74F157"-pin 5 and U7-pin 22.
- Add a wire between "74F157"-pin 7 and U4-pin 9.
- Add a wire between "74F157"-pin 9 and U4-pin 2.
- Engrave the character C in the RS232-C p.c. board, next to the code-number: P/N 940-0552 REV
- Scratch the old rev. indication (if present).

ROM emulator pod control:
The Rom emulator pod is controlled via a serial link which is under control of the microprocessor.
Buffer U13 transfers control signals (CTL0, CTL1) and pod select signals (SEL0, SEL1) to the ROM emulator pod. These signals are generated via the upper half of port A in U12.
Buffer U13 also transfers the clock signal (RCLK) -for the inputbuffers in the pod-, and the serial data that goes to the pod or comes from the pod (DDWN and SELDAT respectively).
The data that has to be downloaded or uploaded to or from the ROM emulator pod is loaded into shift register U3 via port B of U7.
A high signal LOAD loads data from the microprocessor into the shift register (U3) on the next clock pulse (on pin 12). The data is then shifted out to the pod (DDWN) on the next 8 clock pulses (LOAD is low).
A low signal LOAD permits the pod to shift data (DUP) into the shift register and then the microprocessor can read this data.

The clock signal (RCLK) for the pod and shift register is derived from the microprocessor clock via clock divider U1 (URTCK).
For loading one byte of information into the pod, 8 clock pulses are needed to fill the input shift registers in the pod (clocksignal RCLK).
For this, the uP resets U4 (via lower part of port A) when a data byte is ready in U3 or when a next data byte can be read from trhe pod.
U4 then counts 8 clock pulses and stops itself via the terminal count output.
For the next byte, the counter has to be reset again.
For loading one byte of data into U3 (via port B of U7) counter U4 is first loaded with 1110 (via lower part of port A, pin 22) and then counts 1 clock pulse before it stops itself via the terminal count output. This clock pulse loads data from port B into shift register U3.

LIST OF SIGNAL NAMES (diagram 22)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	22
A 8	Address line 8	2	22
A 9	Address line 9	2	22
A10	Address line 10	2	22
A11	Address line 11	2	22
A12	Address line 12	2	22
A13	Address line 13	2	22
A14	Address line 14	2	22
A15	Address line 15	2	22
A15*	Address line 15	22	22
AD0	Address/data line 0	2	22
AD1	Address/data line 1	2	22
AD2	Address/data line 2	2	22
AD3	Address/data line 3	2	22
AD4	Address/data line 4	2	22
AD5	Address/data line 5	2	22
AD6	Address/data line 6	2	22
AD7	Address/data line 7	2	22
ALE	Address latch enable	2	22
BRD*	Buffered dear signal	22	22
BSELDAT	Buffered serial data up	14	22
CTL0	Control line 0	22	14
CTL1	Control line 1	22	14
DDWN	Data down (to Rom emulator)	22	14,22
DUP	Data up (from rom emulator)	22	22
ECLK	Rom emulator clock	22	14
INT	Interrupt signal	22	22
INTEN*	Interrupt enable	22	22
IO/M*	Input,output/ memory	2	22
LOAD	Load data	22	22
OPINT*	Option interrupt	22	1,2,6
OPSEL*	Option select line	3	22
RAMEN*	Enable scratch pad ram	22	22
RD*	Read signal	2	22
READY	Ready	22	1,2,6
RESET OUT	Reset out signal	2	22
ROMEN*	Enable control rom	22	22
RXRDY	Receiver register ready	22	22
S0	Status line 0	2	22
S1	Status line 1	2	22
SEL0	Select line 0	22	14
SEL1	Select line 1	22	14
TXEMPTY	Transmitter register empty	22	22
TXIDIS*	Enable transmitter interrupt	22	22
TYPEN*	Enable buffer for id read	22	22
UARTEN*	Enable uart	22	22
UARTCK	Uart clock	22	22
WR*	Write signal	2	22

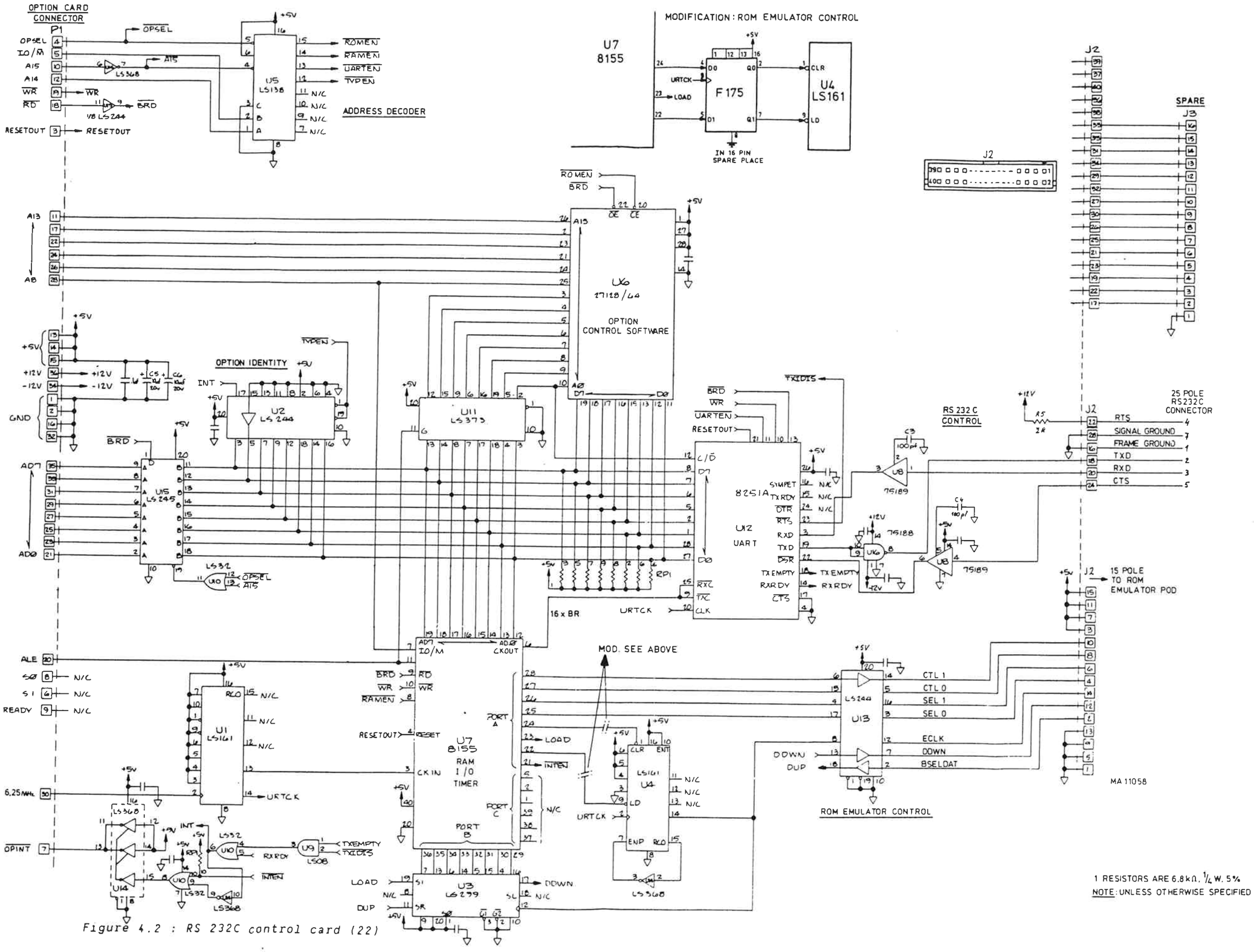


Figure 4.2 : RS 232C control card (22)

4.4 SETUP DATA MEMORY (see figures 4.3 and 4.4)

This option is used to store up to 8 different settings and up to 8K of data into non volatile memory.
Also compare, search and autosequence modes are possible when this board is installed.

NOTE:

This description also covers the setup memory option which is a part of the setup data memory option.
The difference between these options is that the setup data memory has:

- *4 extra EEPROMs (U3, U4, U5 and U6)*
- *1 extra RAM (U2)*
- *different control software (U1)*

Connector P1 connects the setup data memory option to the address, data and control busses of the microprocessor on the capture board (see figure 4.3).
Data and addresslines are first buffered via U16, U17.
The data lines of this option board are only connected to the databus of the microprocessor when this board is selected (signal BRDSEL*).
The lower addresslines are latched in U12 (by means of the ALE pulse).

The option board is selected via signal OPSEL which is one of the three option select lines (OPSEL0....OPSEL2) that come from the microprocessor (U15, see figure 2.7). Because the option board can be in any of the three slots, the select signal is just called OPSEL.
The microprocessor first reads the identity of the option boards in the slots (by reading buffer U11) and then knows which of the three OPSEL0....OPSEL2 lines it has to activate to access the setup data memory option.

Decoder U19 is enabled only when the option board is selected (signal OPSEL) and when address line A15 is high (addresses 8000 and up; see also figure 2.5, memory map).
This decoder selects (8 K blocks)

- bank switch register : U13, by means of signal SELREG* : I/O mapped.
- "identity buffer" : U11, by means of signal BRDTYPE*: I/O mapped.
- PROM U1 : U1, by means of signal ROM* :memory mapped.
- reference RAM : U2, by means of signal RAM1* :memory mapped.
- one extra 8K block

The extra 8 K block is further decoded by U14 (2 K blocks) which selects:

- -EEPROMS1...5 : U3, U4, U5, U6 or U7, by means of signals EEPROM1*...EEPROM5*: memory mapped
- -scratch pad RAM : U8, by means of signal RAM2 : memory mapped.

Bank select buffer U13 is used to select the different EEPROMs which are located on the same memory location (signal BANK, from U13 to U14).
When BANK = 0 : then EEPROMs U3, U4 and U7 are selected.
When BANK = 1 : then EEPROMs U5, U6 and U7 are selected.
Signal RA14 is used as bank select signal for the PROM that contains the control software (U1). This select signal is only used to switch-off PROM U1 in case it is a 27256 and the EEPROMs have to be selected. Until now this PROM has been a 27128 so this select signal is not yet used.

Via buffer U15, the microprocessor can read the status of the bankselection, the kind of EEPROMs that is used and also the RDY/BUSY* line of the EEPROMs when the INTEL PROMs are used.
In case of INTEL EEPROMs the microprocessor reads RDY/BUSY*. When it is high, the microprocessor can write new data to the PROMs.

The EEPROM can either be INTEL or XICOR PROMs. To select this, jumper W1 can be closed or opened, however only XICOR PROMs are used.
The EEPROMs have a power-down protection. This circuit, consisting of U9, Q1 and associated components, keeps the write line (BWR*) high when the power goes down from 4.5 V to 3.0 V. If the write line is not stable during this interval, it will overwrite the information in the EEPROMs.

LIST OF SIGNAL NAMES (diagram 23)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Oescribes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
6.2016 MHz	Video and uP clock	3	23
A 8	Addressline 8	2	23
A 9	Addressline 9	2	23
A10	Addressline 10	2	23
A11	Addressline 11	2	23
A12	Addressline 12	2	23
A13	Addressline 13	2	23
A14	Addressline 14	2	23
A15	Addressline 15	2	23
AD0	Address/data line 0	2	23
AD1	Address/data line 1	2	23
AD2	Address/data line 2	2	23
AD3	Address/data line 3	2	23
AD4	Address/data line 4	2	23
AD5	Address/data line 5	2	23
AD6	Address/data line 6	2	23
AD7	Address/data line 7	2	23
ALE	Address latch enable	2	23
ASD0	Address line 0	23	24
ASD1	Address line 1	23	24
ASD2	Address line 2	23	24
ASD3	Address line 3	23	24
ASD4	Address line 4	23	24
ASD5	Address line 5	23	24
ASD6	Address line 6	23	24
ASD7	Address line 7	23	24
BA 8	Buffered address line 8	23	24
BA 9	Buffered address line 9	23	24
BA10	Buffered address line 10	23	24
BAD0	Buffered address/data line 0	23	24
BAD1	Buffered address/data line 1	23	24
BAD2	Buffered address/data line 2	23	24
BAD3	Buffered address/data line 3	23	24
BAD4	Buffered address/data line 4	23	24
BAD5	Buffered address/data line 5	23	24
BAD6	Buffered address/data line 6	23	24
BAD7	Buffered address/data line 7	23	24
BANK	Bank select	23	23
BRD*	Buffered read signal	23	23
BRDSEL*	Board selection	23	23
BRDTYPE*	Enable id buffer	23	23
BWR*	Buffered write signal	23	23,24
EEPROM1*	Enable EEPROM 1	23	24
EEPROM2*	Enable EEPROM 2	23	24
EEPROM3*	Enable EEPROM 3	23	24
EEPROM4*	Enable EEPROM 4	23	24
EEPROM5*	Enable EEPROM 5	23	24

LIST OF SIGNAL NAMES (diagram 23, continued)

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
IO*/M	Input/output/memory	23	24
IO/M*	Input,output/ memory	2	23
OPINT*	Option interrupt	23	1,2,6
OPSEL*	Option select; slot 0,1 or 2	3	23
RA14	Address line 14	23	23
RAM1*	Enable reference ram	23	23
RAM2*	Enable scratch pad ram	23	23
RD*	Read signal	2	23
RDY/BUSY*	Ready/Busy signal	23	24
READY	Ready	23	1,2,6
RESET OUT	Reset out signal	2	23
ROM*	Enable control rom	23	23
S0	Status line 0	2	23
S1	Status line 1	2	23
SELREG*	Select bank switch register	23	23
WR*	Write signal	2	23

LIST OF SIGNAL NAMES (diagram 24)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destignation (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
ASD0	Address line 0, setup/data	23	24
ASD1	Address line 1, setup/data	23	24
ASD2	Address line 2, setup/data	23	24
ASD3	Address line 3, setup/data	23	24
ASD4	Address line 4, setup/data	23	24
ASD5	Address line 5, setup/data	23	24
ASD6	Address line 6, setup/data	23	24
ASD7	Address line 7, setup/data	23	24
BA 8	Buffered address line 8 setup	23	24
BA 9	Buffered address line 9 setup	23	24
BA10	Buffered address line 10 setup	23	24
BAD0	Buffered address/data line 0 setup	23	24
BAD1	Buffered address/data line 1 setup	23	24
BAD2	Buffered address/data line 2 setup	23	24
BAD3	Buffered address/data line 3 setup	23	24
BAD4	Buffered address/data line 4 setup	23	24
BAD5	Buffered address/data line 5 setup	23	24
BAD6	Buffered address/data line 6 setup	23	24
BAD7	Buffered address/data line 7 setup	23	24
BWR*	Buffered write signal, setup/data	23	24
EEPROM1*	Enable EEPROM1	23	24
EEPROM2*	Enable EEPROM2	23	24
EEPROM3*	Enable EEPROM3	23	24
EEPROM4*	Enable EEPROM4	23	24
EEPROM5*	Enable EEPROM5	23	24
RDY/BUSY*	Ready/Busy signal, setup/data	23	24

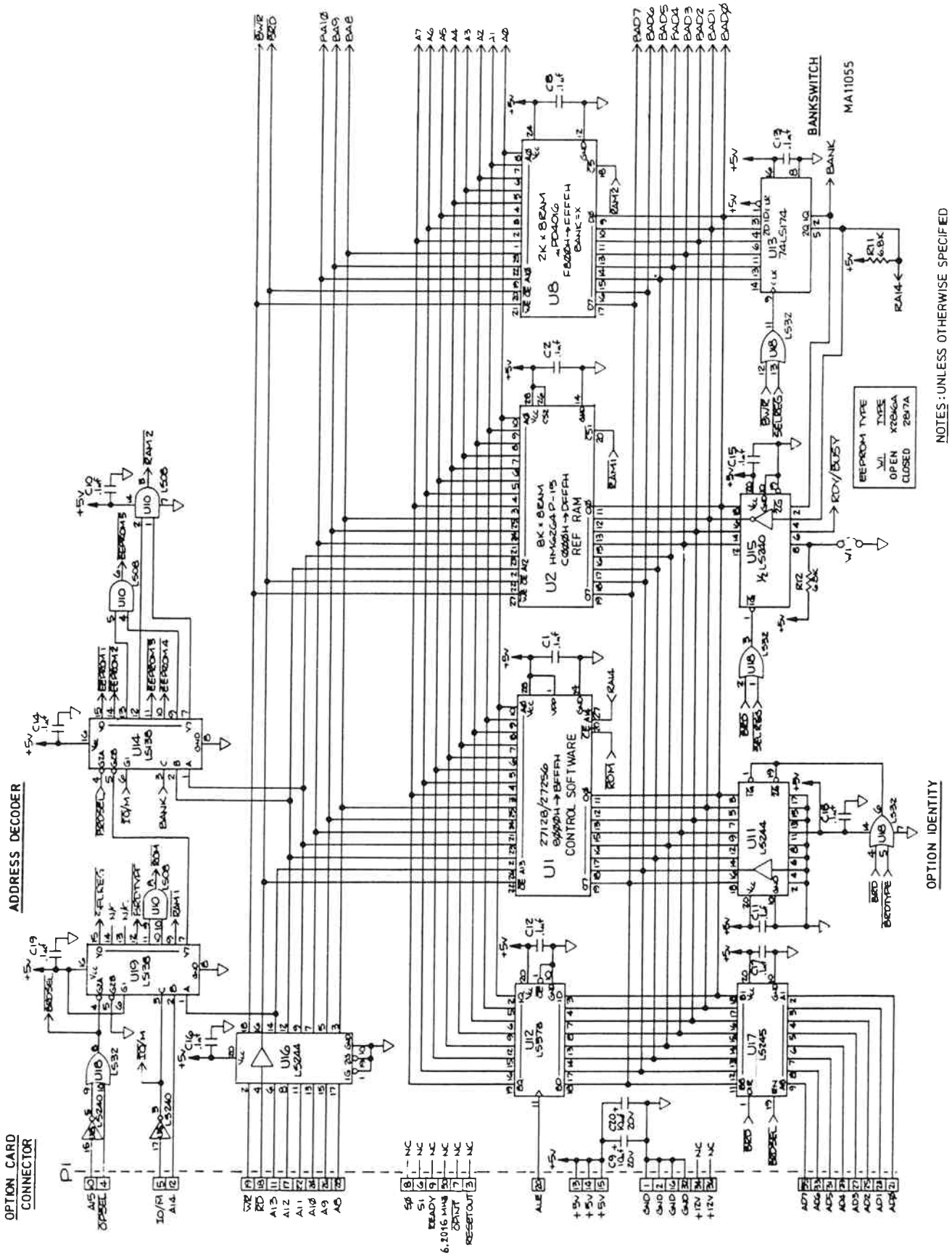


Figure 4.3 : Setup data memory (23)

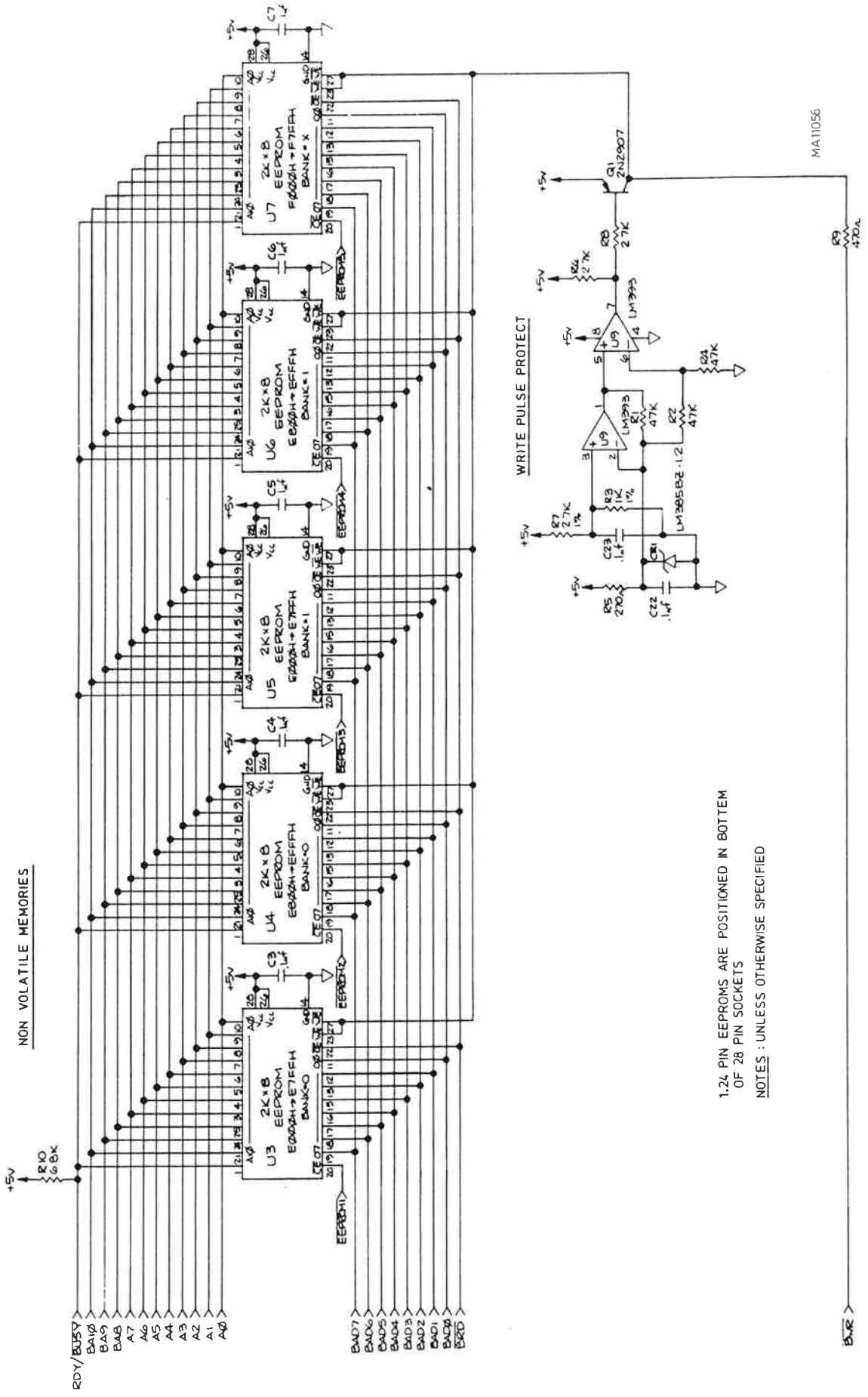


Figure 4.4 : Setup data memory; EFPROMs (24)

4.5 COMPOSITE VIDEO OUTPUT (see figure 4.5)

This option is used to generate a composite video signal which can be used to connect an external monitor, or for example a video printer.

The video output **MUST** be installed in the service workshop, and is certainly not user installable (see section 7.3 for installation instructions).

The video interface combines the following signals into one composite video signal:

VRTC	(Vertical retrace)
HRTC	(Horizontal retrace)
VIDEO	(Video signal from microcomputer-video interfavce)

The output signal is a composite video signal which can be used on 50 Hz monitors, or for example on a video printer.

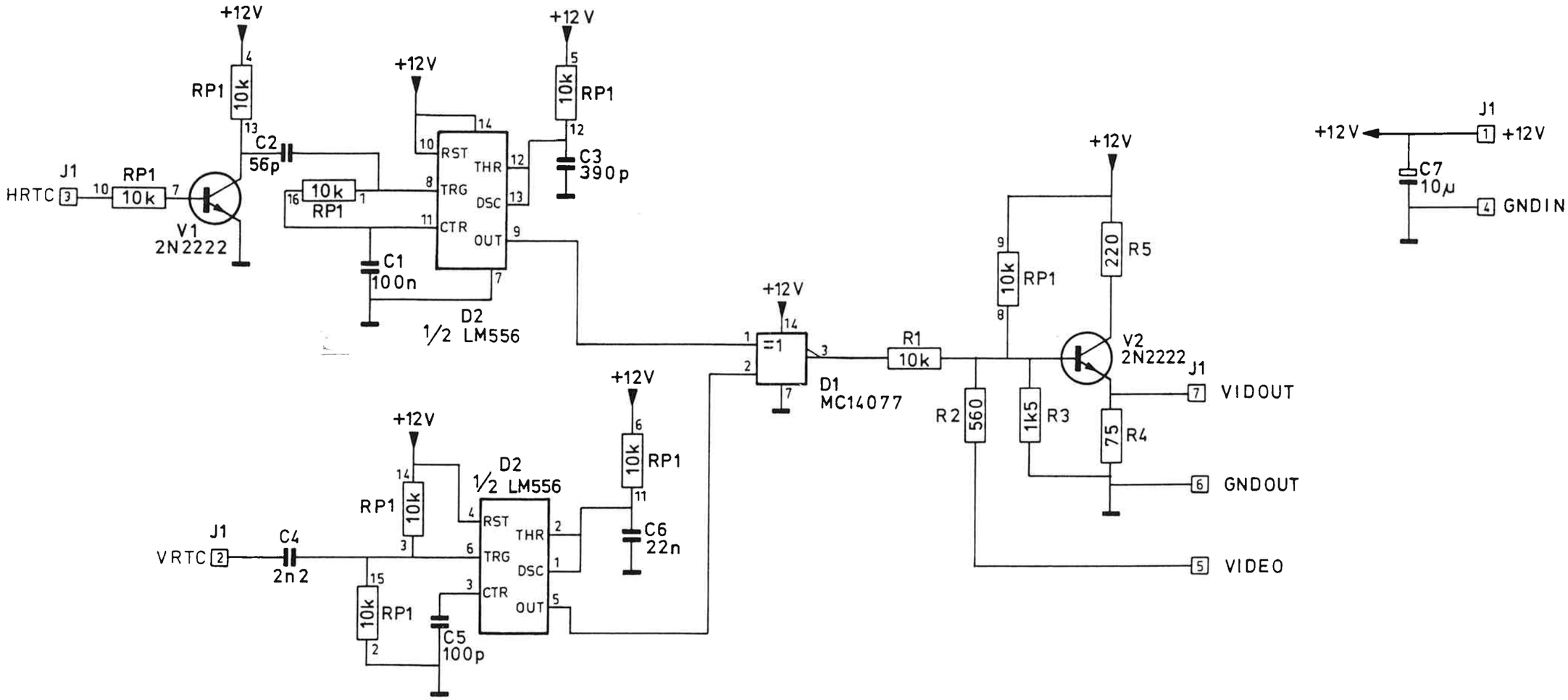
The vertical and horizontal retrace signals, both pass a one-shot (U2), before they are combined into one synchronisation signal (in U1).
The video signal, generated by the video interface of the microcomputer, is added to the synchronisation signal in the output stage (Q2).
After the output stage, there is a composite video signal available.
This output stage has a 75 ohm output impedance.

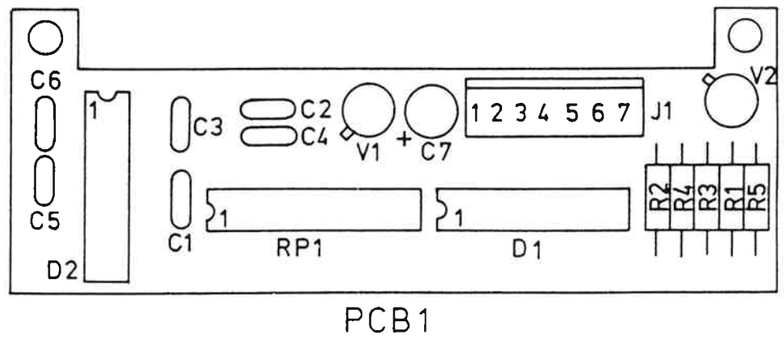
NOTE: U2 (LM556) is a selected part. Only tested parts can be used!!

LIST OF SIGNAL NAMES (diagram 31)

SIGNAL NAME : Is the signal name that is used in the diagrams. A * indicates that it is an inverted signal; in the diagrams these are indicated with a horizontal bar above the signal name.
DESCRIPTION : Describes the meaning of each signal name
GENERATED ON: The source (diagram number) of each signal name
USED ON : The destination (diagram number) of each signal name.
A ? indicates that the source cannot be defined (for example one signalname can come from different pods, but only one can be connected).
A 'BD' indicates that it is a bidirectional signal.

SIGNALNAME	DESCRIPTION	GENERATED ON DIAGRAM	USED ON DIAGRAM
HRTC	Horizontal retrace	2	31
VRTC	Vertical retrace	2	31
VIDEO	Video signal	2	31
VIDOUT	Composite video out	31	BNC plug
GNDOUT	Ground signal out	31	BNC plug





PCB1

MA11176

Figure 4.5 : Video output (31)

4.5 SPARE PARTS, OPTIONS

This list contains all components which are not standard.

The p.c. boards for the options are not available from Concern Service. When, however, you need a spare p.c. board for a particular option, you can order it via the commercial department.

Proms with option software are also not available from Concern Service. When you want to order option software, contact the DTE Supply Centre Service group.

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BUILDING TQ V-2
EINDHOVEN

POSITION	DESCRIPTION	ORDERING CODE
DISA ROM BOARD		
Integrated circuits:		
U17	74LS32	5322 209 85311
U12,18	74LS138	5322 209 85647
U14	74LS240	5322 209 85862
U10,15	74LS244	5322 209 86017
U16	74LS245	5322 209 86225
U13	74F379	5322 209 82887
U9	M58725P	5322 209 82855
U11	74LS373	5322 209 86062
Various:		
RP1	RES. NETW. 6.8K	5322 111 90834
RS 232C CONTROL CARD		
Integrated circuits:		
U10	74LS32	5322 209 85311
U5	74LS138	5322 209 85647
U1,4	74LS161	5322 209 85915
U2,13	74LS244	5322 209 86017
U15	74LS245	5322 209 86225
U3	74LS299	5322 209 86002
U14	74LS368	4822 209 80448
U11	74LS373	5322 209 86062

APPENDIX D

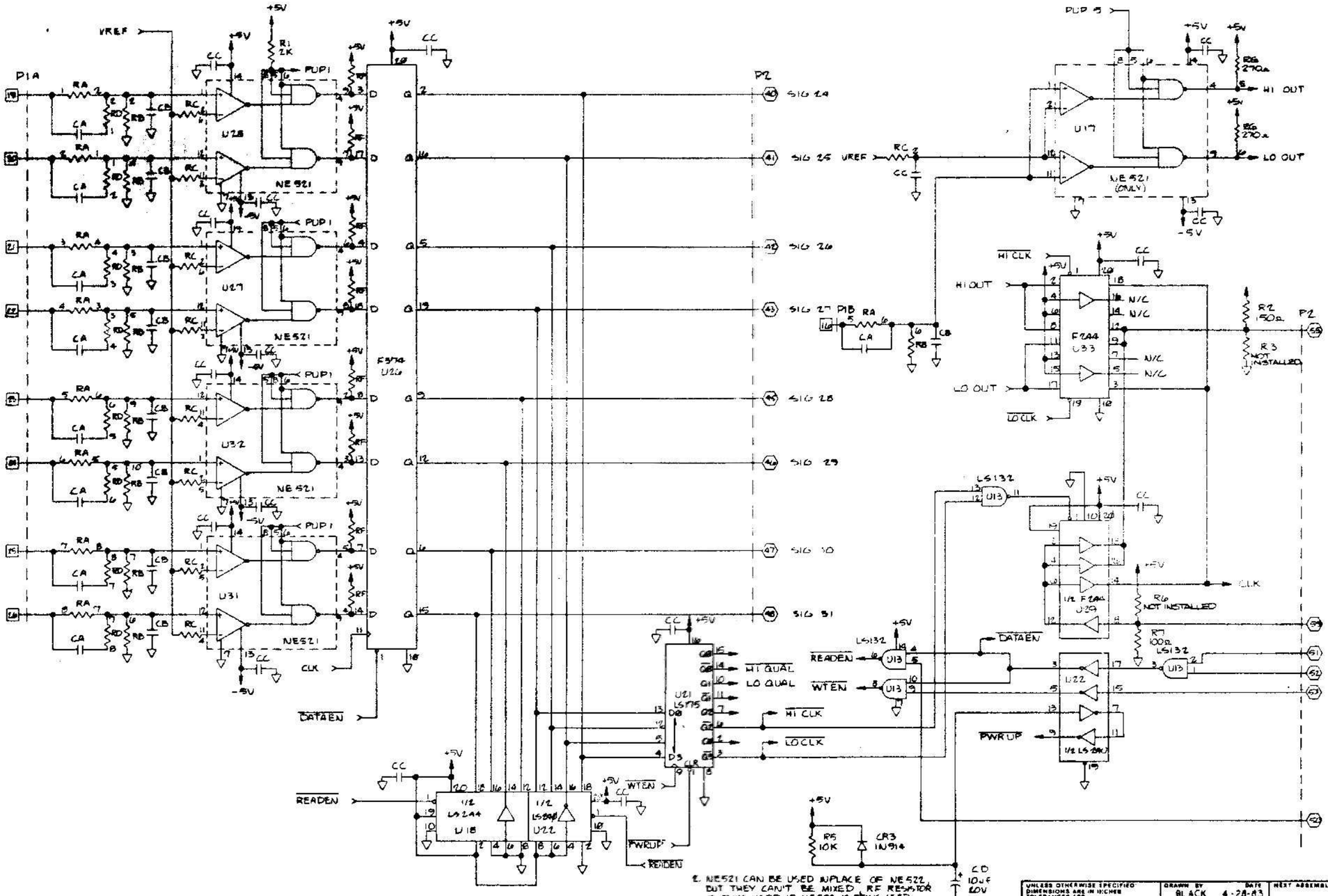
Program listing of 8085/Z80 demo unit.

```
1                                       NAME    MLTEST
2       0000                            ASEG
3                               ;
4                               ;       THIS HIGHLY COMPLICATED PROGRAM WILL PROBABLY TAKE THE EXPERIENCED
5                               ;       PROGRAMMER SEVERAL HOURS TO COMPREHEND.  PRESS SWITCH 1, GOTO STATE 1.
6                               ;       PRESS SWITCH 2, GOTO STATE 2.  PRESS EITHER SWITCH ONCE AND THE OTHER
7                               ;       SWITCH TWICE AND GOTO STATE 0.
8                               ;
9                               ;       BREAKPOINTS FOR STATES:
10                              ;
11                              ;               STATE0 -   0H
12                              ;               STATE1 - 100H
13                              ;               STATE2 - 200H
14                              ;
15                              ;       STATE 0
16                              ;
17      0000                            ORG     0
18                              ;
19 0000 F3              STATE0: DI                      ;DISABLE INTERRUPTS
20 0001 21      AAAA            LXI     H,0AAAAH        ;MAKE SURE ALL BITS GO DIFFERENT WAYS
21 0004 36      04              MVI     M,H
22 0006 21      5555            LXI     H,5555H
23 0009 36      04              MVI     M,H
24 000B DB      00              IN      0               ;READ INPUT SWITCH PORT
25 000D E6      01              ANI     1               ;MASK SWITCH 1
26 000F CA      0035            JZ      A10             ;IF PRESSED THEN JUMP ELSE
27 0012 DB      00              IN      0               ;READ INPUT SWITCH PORT
28 0014 E6      02              ANI     2               ;MASK SWITCH 2
29 0016 C2      0080            JNZ     MULTA           ;IF NOT PRESSED THEN JUMP ELSE
30 0019 21      03E8            LXI     H,1000          ;DEBOUNCE SWITCH
31 001C 74              A5:     MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
32 001D 75                      MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
33 001E 2B                      DCX     H               ;DECREMENT CTR
34 001F 7C                      MOV     A,H             ;IS DEBOUNCE TIME OVER
35 0020 B5                      ORA     L
36 0021 C2      001C            JNZ     A5              ;IF NOT THEN LOOP ELSE
37 0024 DB      00              IN      0               ;IS SWITCH STILL PRESSED?
38 0026 E6      02              ANI     2
39 0028 C2      0000            JNZ     STATE0          ;IF NOT THEN IGNORE SWITCH ELSE
40 002B DB      00      A8:     IN      0               ;WAIT FOR SWITCH TO BE RELEASED
41 002D E6      02              ANI     2
42 002F CA      002B            JZ      A8              ;LOOP IF STILL PRESSED ELSE
43 0032 C3      0200            JMP     STATE2          ;JUMP TO STATE2
44                              ;
45 0035 21      03E8    A10:    LXI     H,1000          ;DEBOUNCE SWITCH
46 0038 74              A15:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
47 0039 75                      MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
48 003A 2B                      DCX     H               ;DECREMENT CTR
49 003B 7C                      MOV     A,H             ;IS DEBOUNCE TIME OVER
50 003C B5                      ORA     L
51 003D C2      0038            JNZ     A15             ;IF NOT THEN LOOP ELSE
52 0040 DB      00              IN      0               ;IS SWITCH STILL PRESSED?
53 0042 E6      01              ANI     1
54 0044 C2      0000            JNZ     STATE0          ;IF NOT THEN IGNORE SWITCH ELSE
55 0047 DB      00      A18:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
56 0049 E6      01              ANI     1
57 004B CA      0047            JZ      A18             ;LOOP IF STILL PRESSED ELSE
```

```
 1 004F   C3     0100            JMP     STATE1          ;JUMP TO STATE1
 2                        ;
 3                        ;       8X8 MULTIPLY. OPERANDS IN H & E. ANSWER IN HL
 4                        ;
 5        0080                    ORG     80H
 6                        ;
 7 0080   26     55      MULTA:  MVI     H,055H          ;SET OPERANDS
 8 0082   1E     AA              MVI     E,0AAH
 9 0084   3F     08              MVI     A,8             ;SET LOOP CTR
10 0086   2E     00              MVI     L,0             ;PUT MULTIPLIER IN HL
11 0088   55                     MOV     D,L             ;ZERO D
12 0089   29             MULT1:  DAD     H               ;SHIFT MULTIPLIER AND ANSWER TO LEFT
13 008A   74                     MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
14 008B   75                     MOV     M,L
15 008C   D2     0092            JNC     MULT2           ;IF NO MULTIPLIER BIT SHIFTED OUT THEN JUMP ELSE
16 008F   19                     DAD     D               ;AND MULTIPLICAND TO ANSWER
17 0090   74                     MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
18 0091   75                     MOV     M,L
19 0092   3D             MULT2:  DCR     A               ;DECREMENT LOOP CTR
20 0093   77                     MOV     M,A             ;PUT LOOP CTR OUT ON BUS
21 0094   C2     0089            JNZ     MULT1           ;LOOP IF NOT DONE ELSE
22 0097   C3     0000.           JMP     STATE0          ;LOOP AND CHECK FOR SWITCHES AGAIN
23                       ;
24                       ;       STATE 1
25                       ;
26       0100                    ORG     100H
27                       ;
28 0100   DB     00      STATE1: IN      0               ;READ INPUT SWITCH PORT
29 0102   E6     01              ANI     1               ;MASK SWITCH 1
30 0104   CA     012A            JZ      A23             ;IF PRESSED THEN JUMP ELSE
31 0107   DB     00              IN      0               ;READ INPUT SWITCH PORT
32 0109   E6     02              ANI     2               ;MASK SWITCH 2
33 010B   C2     0180            JNZ     MULTR           ;IF NOT PRESSED THEN JUMP ELSE
34 010E   21     03E8            LXI     H,1000          ;DEBOUNCE SWITCH
35 0111   74             A19:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
36 0112   75                     MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
37 0113   2B                     DCX     H               ;DECREMENT CTR
38 0114   7C                     MOV     A,H             ;IS DEBOUNCE TIME OVER
39 0115   B5                     ORA     L
40 0116   C2     0111            JNZ     A19             ;IF NOT THEN LOOP ELSE
41 0119   DB     00              IN      0               ;IS SWITCH STILL PRESSED?
42 011B   E6     02              ANI     2
43 011D   C2     0100            JNZ     STATE1          ;IF NOT THEN IGNORE SWITCH ELSE
44 0120   DB     00      A20:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
45 0122   E6     02              ANI     2
46 0124   CA     0120            JZ      A20             ;LOOP IF STILL PRESSED ELSE
47 0127   C3     0200            JMP     STATE2          ;JUMP TO STATE2
48                       ;
49 012A   21     03E8    A23:    LXI     H,1000          ;DEBOUNCE SWITCH
50 012D   74             A25:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
51 012E   75                     MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
52 012F   2B                     DCX     H               ;DECREMENT CTR
53 0130   7C                     MOV     A,H             ;IS DEBOUNCE TIME OVER
54 0131   B5                     ORA     L
55 0132   C2     012D            JNZ     A25             ;IF NOT THEN LOOP ELSE
56 0135   DB     00              IN      0               ;IS SWITCH STILL PRESSED?
57 0137   E6     01              ANI     1
```

```
 1 0139   C2    0100          JNZ     STATE1          ;IF NOT THEN IGNORE SWITCH ELSE
 2 013C   DB    00    A28:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
 3 013E   E6    01            ANI     1
 4 0140   CA    013C          JZ      A28             ;LOOP IF STILL PRESSED ELSE
 5 0143   C3    0000          JMP     STATE0          ;JUMP TO STATE0
 6                    ;
 7                    ;       8X8 MULTIPLY. OPERANDS IN H & E. ANSWER IN HL
 8                    ;
 9        0180                ORG     180H
10                    ;
11 0180   26    34    MULTB:  MVI     H,034H          ;SET OPERANDS
12 0182   1E    56            MVI     E,056H
13 0184   3E    08            MVI     A,8             ;SET LOOP CTR
14 0186   2E    00            MVI     L,0             ;PUT MULTIPLIER IN HL
15 0188   55                  MOV     D,L             ;ZERO D
16 0189   29          MULT1B: DAD     H               ;SHIFT MULTIPLIER AND ANSWER TO LEFT
17 018A   74                  MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
18 018B   75                  MOV     M,L
19 018C   D2    0192          JNC     MULT2B          ;IF NO MULTIPLIER BIT SHIFTED OUT THEN JUMP ELSE
20 018F   19                  DAD     D               ;ADD MULTIPLICAND TO ANSWER
21 0190   74                  MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
22 0191   75                  MOV     M,L
23 0192   3D          MULT2B: DCR     A               ;DECREMENT LOOP CTR
24 0193   77                  MOV     M,A             ;PUT LOOP CTR OUT ON BUS
25 0194   C2    0189          JNZ     MULT1B          ;LOOP IF NOT DONE ELSE
26 0197   C3    0100          JMP     STATE1          ;LOOP AND CHECK FOR SWITCHES AGAIN
27                    ;
28                    ;       STATE 2
29                    ;
30        0200                ORG     200H
31                    ;
32 0200   DB    00    STATE2: IN      0               ;READ INPUT SWITCH PORT
33 0202   E6    01            ANI     1               ;MASK SWITCH 1
34 0204   CA    022A          JZ      A40             ;IF PRESSED THEN JUMP ELSE
35 0207   DB    00            IN      0               ;READ INPUT SWITCH PORT
36 0209   E6    02            ANI     2               ;MASK SWITCH 2
37 020B   C2    0280          JNZ     MULTC           ;IF NOT PRESSED THEN JUMP ELSE
38 020E   21    03E8          LXI     H,1000          ;DEBOUNCE SWITCH
39 0211   74          A35:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
40 0212   75                  MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
41 0213   2B                  DCX     H               ;DECREMENT CTR
42 0214   7C                  MOV     A,H             ;IS DEBOUNCE TIME OVER
43 0215   B5                  ORA     L
44 0216   C2    0211          JNZ     A35             ;IF NOT THEN LOOP ELSE
45 0219   DB    00            IN      0               ;IS SWITCH STILL PRESSED?
46 021B   E6    02            ANI     2
47 021D   C2    0200          JNZ     STATE2          ;IF NOT THEN IGNORE SWITCH ELSE
48 0220   DB    00    A38:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
49 0222   E6    02            ANI     2
50 0224   CA    0220          JZ      A38             ;LOOP IF STILL PRESSED ELSE
51 0227   C3    0000          JMP     STATE0          ;JUMP TO STATE0
52                    ;
53 022A   21    03E8  A40:    LXI     H,1000          ;DEBOUNCE SWITCH
54 022D   74          A45:    MOV     M,H             ;PUT MSB OF CTR ON ADDRESS BUS FOR DISASSEMBLY
55 022E   75                  MOV     M,L             ;PUT LSB OF CTR ON ADDRESS BUS
56 022F   2B                  DCX     H               ;DECREMENT CTR
57 0230   7C                  MOV     A,H             ;IS DEBOUNCE TIME OVER
```

```
 1 0231  B5                      ORA     L
 2 0232  C2      022D            JNZ     A45             ;IF NOT THEN LOOP ELSE
 3 0235  DB      00              IN      0               ;IS SWITCH STILL PRESSED?
 4 0237  E6      01              ANI     1
 5 0239  C2      0200            JNZ     STATE2          ;IF NOT THEN IGNORE SWITCH ELSE
 6 023C  DB      00      A48:    IN      0               ;WAIT FOR SWITCH TO BE RELEASED
 7 023E  E6      01              ANI     1
 8 0240  CA      023C            JZ      A48             ;LOOP IF STILL PRESSED ELSE
 9 0243  C3      0100            JMP     STATE1          ;JUMP TO STATE1
10                      ;
11                      ;
12                      ;       8X8 MULTIPLY. OPERANDS IN H & E. ANSWER IN HL
13                      ;
14      0280                    ORG     280H
15                      ;
16 0280  26      DC     MULTC:  MVI     H,0DCH          ;SET OPERANDS
17 0282  1E      23              MVI     E,023H
18 0284  3E      08              MVI     A,8             ;SET LOOP CTR
19 0286  2E      00              MVI     L,0             ;PUT MULTIPLIER IN HL
20 0288  55                      MOV     D,L             ;ZERO D
21 0289  29              MULT1C: DAD     H               ;SHIFT MULTPLIER AND ANSWER TO LEFT
22 028A  74                      MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
23 028B  75                      MOV     M,L
24 028C  D2      0292            JNC     MULT2C          ;IF NO MULTIPLIER BIT SHIFTED OUT THEN JUMP ELSE
25 028F  19                      DAD     D               ;ADD MULTIPLICAND TO ANSWER
26 0290  74                      MOV     M,H             ;PUT PARTIAL ANSWER ON BUS
27 0291  75                      MOV     M,L
28 0292  3D              MULT2C: DCR     A               ;DECREMENT LOOP CTR
29 0293  77                      MOV     M,A             ;PUT LOOP CTR OUT ON BUS
30 0294  C2      0289            JNZ     MULT1C          ;LOOP IF NOT DONE ELSE
31 0297  C3      0200            JMP     STATE2          ;LOOP AND CHECK FOR SWITCHES AGAIN
32                      ;
33                              END
```



2. NE521 CAN BE USED INPLACE OF NE522, BUT THEY CAN'T BE MIXED. RF RESISTOR IS ONLY USED IF NE522 IS BEING USED.

3. COMPONENT VALUES:
RA = 82K, RB = 15K, RC = 15K, RD = 2.2K, RE = 1.2K, RF = 220
CA = 6.8pF, CB = 27pF, CC = .1μF, 50V, CD = 10μF, 20V

NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES : .XX ± : .XXX :	DRAWN BY BLACK DATE 4-28-83	NEXT ASSEMBLY
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TITLE: ML4100: LP320, GENL. PURPOSE LOGIC PCD

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