Personal Logic Analyzer
Incl. Options and Accessories
PM 3632

Operating manual Edition 2.2

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1. INTRODUCTION

1.1 GENERAL

The PM 3632 Logic Analyzer provides full-featured logic analysis for the debugging and troubleshooting of digital and micro-processor-based products, including complex triggering with list, timing, and (optionally) microprocessor disassembly displays.

Its basic function is to capture (record) the digital data on several signal lines, repetitively, and to do this synchonously or asynchronously with the clock of the system under test. High-speed, asynchronous operation is a powerful aid when solving hardware logic timing problems, while low-speed, synchronous operation is useful for debugging software.

The PM 3632 operates at speeds of up to 100 MHz, at data widths of up to 32 channels, and at a memory depth of up to 8000 samples per channel. At 100 MHz, the maximum number of channels is 4; when using 32 channels, the maximum speed is 12.5 MHz; and the maximum memory depth of 8000 samples per channel is available only when using up to 4 channels.

Data and clock qualifiers can be used, as well as trigger delay of up to 50,000 clocks. Data qualification is available only with 32-channel operation.

The optional ROM Emulator Module provides in-circuit emulation of 2716, 2732, 2764 and 27128 PROMs and immediate code patches, and an RS-232C interface provides for code downloading or uploading.

The PM 3632 contains a 5-inch, green-screen CRT which displays up to twelve channels of timing diagrams (with labelling) and has cursors for time-measurements.
The list display can be formatted and reformatted to achieve almost any conceivable digit combination in several number bases : ASCII, binary, octal, decimal, or hexadecimal.

Other options are micro-processor pods with one-clip connection to most popular micro-processors ; the resulting disassembly display shows mnemonics for the various instruction and data sequences.

Four trigger words are available, and can be defined in binary, octal, decimal, or hexadecimal number base. These four words can be combined to form the trigger condition in many different ways. Nineteen trigger sequences are predefined and selectable, and the user may define his own sequence as well. All predefined sequences are available in the 32-channel mode, but these sequences are somewhat more limited in the other modes.

The PM 3632 has been designed for simple set-up and ease of operation. All set-up- and display screens contain complete prompting information which is self-explanatory for most situations. This enables the user to make productive use of this logic analyzer with a minimum of experience and, we hope, only infrequent reference to this manual.

The instrument has been designed and tested according to IEC Publication 348 for Class 1 instruments, and has been supplied in a safe condition. The present Operating Manual contains information and warnings which should be followed by the purchaser to ensure safe operation and to maintain the instrument in a safe condition.

1.2 PM 3632 SYSTEM FAMILY

PODS

PM 8860	32-channel Logic Pod (standard accessory)
PM 8862	4-channel High-speed Pod
PM 8863	Standard Bus Pod
PM 8864	Rom Emulator Pod
PM 8865	Micro-processor Pod for 8085, 8031, 8032, 8035, 8039 and 8040
PM 8866	Micro-processor Pod for 6800, 6802 and 6808
PM 8867	Micro-processor Pod for 6809 and 6809E
PM 8868	Micro-processor Pod for 6502, 6512, 65C02, 65C102 and 65C112
PM 8869	Micro-processor Pod for Z80 and Z80A/B/C
PM 8870	Micro-processor Pod for NSC800
PM 8874	Micro-processor Pod for 68000/68010
PM 8876	Micro-processor Pod for 8086/8088

Above specified Micro-processor Pods can be used for Disassembly.

OPTIONS

PM 8811	Serial Data Pod
PM 8880/00	Rom Emulator Module *
PM 8880/20	RS-232C Communication Card
PM 8880/30	Disassembly Rom Board
PM 8880/40	Set-up Memory
PM 8880/50	Set-up + Data Memory (can be used for data comparison)
PM 8880/80	Video Output Interface
PM 8883/00	System software rel. L
PM 8884/00	System software rel. L (french screen text)

* The PM 8880/00 Rom Emulator Module consists of:
  -PM 8864 Rom Emulator Unit Pod and
  -PM 8880/20 RS-232C Communication Card.

POD CONNECTING MATERIAL

PM 8882/10	8-channel Probe input wire set *
PM 8882/30	24-channel Probe input wire set *
PM 8882/50	Probe wire set (5 pieces) *
PM 8882/60	Test clip for 40-pin micro-processors

* These sets have disconnectable test hooks

1.3 SYSTEM SPECIFICATIONS

This specification applies to a PM 3632 Analyzer provided with standard Logic Pod PM 8860 unless otherwise stated.

Properties expressed in numerical values with stated tolerances are guaranteed for ambient temperatures of +5 deg.C...+40 deg.C unless stated otherwise.
Numerical values without tolerances are typical and represent the characteristics of an average instrument.
This specification is valid after the instrument has been switched-on for at least 15 minutes.

1.3.1 PM 3632 LOGIC ANALYZER

DATA INPUT

Input width	: 4, 8, 16 or 32 bits. The input width is also referred to as number of channels.
Pod inputs	
Sensitivity	: + and -600 mV centered around threshold
Input voltage	: + or -16 V (operating) + or -20 V (absolute rating)
Threshold	: TTL or Variable Variable ranges from +9 V to -9 V.
Input impedance	: 100 kohm//6 pF

DATA RECORDING CLOCK

Internal (asynchronous)	
Rate	: 5 Hz...100 MHz
External (synchronous)	
Data set-up time	: 5 nsec max.
Data hold time	: 1 nsec max.
Clock period	: 14 nsec min.
Pulse width	: 7 nsec min.
Clock edge	: Positive or negative (external clock only)
Clock qualifier	: 1 (external clock only) Qualifier input data same as for the data inputs.
Max clock rate	: Depending on the recording width, see following list.

Number of Channels	Internal	External
4	100 MHz	70 MHz
8	50 MHz	50 MHz
16	25 MHz	25 MHz
32	12.5 MHz	12.5 MHz

TRIGGERING

Trigger modes : Sequential or Combinational

Trigger words/events : Four

Trigger word width : 32 bits maximum (consistent with the number of channels)

Selectable trigger sequences : 19 pre-defined and 1 user-defined.

Predefined : 0..9
A..F
f1..f3
User-defined: f4

The number of trigger sequences being limited by the number of channels, see following list:

Number of Channels	Available Trigger Sequences
4	0, 1, 2, and 3
8	0, 1, 2, and 3
16	0, 1, and 4
32	All (incl. user-defined)

Trigger Delay : 0...50,000 clock samples

DATA QUALIFICATION (32-bit mode only)

Qualification Modes : State and Combinational

State : Qualification words enable or disable data recording, thus blocks of data to be recorded can be defined.

Combinational : Records only those words which:
1) match qualification words, or
2) don't match qualification words.

MEMORY

Memory depth : Depending on the number of channels

Number of Channels	Recording Depth per Channel
4	8000 samples
8	4000 samples
16	2000 samples
32	1000 samples

LIST DISPLAY MODE

Word list : 14 formatted words

Group columns : 8 max

Number base : Binary, octal, hexadecimal, decimal or ASCII
Repeatable in different number bases and group columns.

Selectable bit groupings for each column.

TIMING DISPLAY MODE

Number of timing lines on the display : 12 max (any line may be repeated)

Cursors : One main cursor, and one reference cursor.

Magnification (horizontal) : x1 and x10 (centered around main cursor)

Time measurements
Units : Clock intervals.
-Clock periods with external clock
-Time units with internal clock.

Measured time
Without reference cursor : Distance from trigger to cursor
With reference cursor : Distance from reference- to main cursor

DISASSEMBLY DISPLAY MODE

14-line list showing addresses, operands, data, mnemonics and bus activity.

DATA SCROLLING

Continuous (auto repeat).

Absolute instantaneous cursor positioning at trigger.

Timing display mode	: Left/right shift, slow or fast
List- and disassembly display modes	: Up/down Slow (one sample at a time), or Fast (one screen at a time)

DISPLAY

5-inch, green phosphor CRT

MAINS INPUT

Voltage	: 220 or 240 V ; internally adjustable. (also adaptation to mains voltages of 100, 110, 120, 127, 200 or 250 V is possible) Refer to chapter 7.
Frequency	: 50..60 Hz (not user-selectable)
Power consumption	: 170 W approx.
Mains fuse (in rear panel)	: 100-127V: 2 Amps (delayed) 200-250V: 1 Amp (delayed) 5x20 mm, glass tube (1 pc)

PHYSICAL MEASUREMENTS

Size	: Depth 38 cm Width 30 cm Heigth 13 cm
Weigth	: 9.9 kg

ENVIRONMENTAL

Temperature	: 0-40 deg C operating
Relative humidity	: 5-95%, non-condensing

1.3.2 OPTIONS AND ACCESSORIES

PM 8860 32-CH LOGIC POD

Data input	: Refer to PM 3632 system specification
Input PROBE 0-7 (16 wires)	: Channel 0...7 External clock Clock qualifier Six ground wires
Input PROBE 8-31 (26 wires)	: Channel 8...31 Two ground wires
Threshold voltage	: TTL = 1.4 V VAR = -9...+9 V The threshold voltage can be measured at point 19 of the PROBE 0-7 connector on the Pod. Refer to Fig. 2.1

PM 8862 4-CH HIGH-SPEED POD

Clock frequency	: 100 MHz max. internal clock 75 MHz max. external clock
Threshold	: TTL = 1.4 V or, VAR = -7.9...+7.9 V The threshold voltage can be measured at the two-pole Molex connector connected to this Pod. The contact at the flat end of this connector is ground potential.
Input voltage	: -7.9...+7.9 V max.
Overdrive	: 40 mV
Input impedance	: 50 kohm// 6 pF
Set-up time	: 5 nsec
Hold time	: 0.5 nsec
Glitch capture	: selectable on/off
Minimum detectable glitch	: 40 mV over threshold for 5 nsec.

PM 8863 STANDARD BUS POD

The STANDARD Bus Pod enables to capture bus cycles asynchronously (with the clock from the analyzer), or synchronously (with the external clock).

Modes : STDBUS
STDINT
STD24B

The STANDARD Bus Pod may be inserted into an unoccupied slot on the bus, or it may be used as an extender card.

PM 8864 ROM EMULATOR POD

For Rom Emulation the Analyzer must be provided with:
-PM 8864 Rom Emulator Pod and
-PM 8880/20 RS-232C Communication Card (located inside the Analyzer)

The ROM Emulator emulates one to four Read-Only Memories per Unit, up to a total of 16 Kbytes of memory, and is configurable for 2716, 2732, 2764, or 27128 PROMs.

One or two PM 8864 pods may be used, for a total of 32 Kbytes of emulation memory. Two units can be daisy-chained.
The simulated ROM memory can be uploaded or downloaded, in several popular data transfer formats, to or from other equipment (such as computers/ controllers or PROM programmers) via an RS-232C port on the back panel.
The memory is then displayed on the PM 3632 screen and can be changed directly with front-panel key entries.

PM 8865...8876 MICRO PROCESSOR PODS

These Pods provide one-clip connection to various micro-processors.
These Pods must be used if a disassembler mode has been selected.
The following Pods are currently available:

Pod Type number	Micro-processors supported
PM 8865	Intel 8085, 8031, 8032, 8035, 8039 and 8040
PM 8866	Motorola 6800, 6802 and 6808
PM 8867	Motorola 6809 and 6809E
PM 8868	Rockwell 6502, 6512, 65C02, 65C102 and 65C112
PM 8869	Zilog Z80, Z80A, Z80B and Z80C
PM 8870	NSC800
PM 8874	68000/68010
PM 8876	8086/8088

Threshold: Fixed TTL

PM 8880/00 ROM EMULATOR MODULE

The PM 8880 Rom Emulator Module consists of:

-PM 8864 Rom Emulator Pod
-PM 8880/20 RS-232C Communication Card (located inside the Analyzer)

ROMs supported	: 2716, 2732, 2764 and 27128
ROM socket plugs	: 4 per Pod
Address bus (all ROMs)	: 14 lines, assumed common
Data busses	: 2 8-bits each, independent for 8- or 16-bits targets.
Timing	: Tacc : 200 nsec Tce : 200 nsec Toe : 70 nsec Iol : 2.1 mA Vol : 0.5 V
Data base interface	: RS-232C Uploads/downloads in hex format
Data editing	: From PM 3632 front-panel keys

PM 8880/20 RS-232C COMMUNICATION CARD

Used in conjunction with the Rom Emulator for upload/download of emulation memory.

Other applications are	: Upload/Download system set-up files or reference memory contents, in conjunction with the PM 8880/40/50.

PM 8880/30 DISASSEMBLER ROM BOARD

This board is required for disassembly of micro-processor programms, and can be installed inside the Analyzer.
For each Disassembler a specific Disa Prom must be present on this board.
The Disa Prom is included in delivery with each Micro-processor Pod.
Up to eight different Disa Proms can be located on the Disa Rom board.

PM 8880/40 SET-UP MEMORY

This unit exists of a non-volatile memory which can store upto eight complete system set-up files. Each file can be assigned a 6-character name and a status of 'protected' or 'unprotected'.
Set-up files can be uploaded or downloaded via the PM 8880/20 RS-232C communication Card.
This unit can be installed inside the Analyzer.

PM 8880/50 SET-UP AND DATA MEMORY

This unit exists of a non-volatile memory which can store upto eight complete system set-up files and one complete data memory (RAM) to be used as a reference memory.
The reference memory is referred to as the 'B'-memory. In relation to this the basic analyzer data memory is called the 'A'-memory.

The set-up files storage functions are described under 'Set-up Memory'.
The reference memory can be partitioned into 1, 2, 4, or 8 equal segments. These segments can then be used by the various set-up files, either singly or in the automatic sequence mode. Each saved data segment can be assigned a 6-character name and a status 'protected' or 'unprotected'.
Data segments can be uploaded or downloaded via the PM 8880/20 RS-232C Communication Card.
The unit can be installed inside the Analyzer.

1.4 CONTROLS AND CONNECTIONS

1.4.1 FRONT-PANEL FUNCTIONS

Fig. 1.1 *PM 3632 Front Panel*

INPUT CONNECTOR - For connecting the Pod.

WARNING : DO NOT PLUG OR UNPLUG THE POD CONNECTOR, WHILE THE UNIT IS POWERED UP.

All operating functions are controlled from the front-panel keybaord. All keys will repeat if held down ; use a quick and sure touch to avoid unwanted repeating.

FOUR ARROW KEYS
To move the cursor on set-up screens, and to scroll through the data on display screens.

START AND STOP KEYS
To start and stop data acquisition.
(To turn on the PM 3632, use the POWER Switch on the back panel).

HEXADECIMAL KEYPAD
To set and change recording- and display parameters.

THREE DISPLAY KEYS (TIMING, LIST and DISASM)
To select the data display mode.

EIGHT SET-UP KEYS
To access set-up screens for specifying parameters for data recording and data display formatting, including a special functions key.

FOUR FUNCTION KEYS f1--4
Keys having various functions depending on the selected display, and on the position of the cursor.

CRT SCREEN
To display data and to set-up recording and display parameters.
Any set-up screen may be accessed with only a single keystroke.
Changeable fields are reverse-videoed and the cursor position blinks, the cursor automatically skips over nonchangeable fields.

To change any set-up or operating parameter, simply position the cursor over the selected field, then enter the desired parameter via the keypad. The new parameter (and any other value determined from it) will be updated and displayed. Actual update occurs when the screen or field is exited via the set-up keys or cursor.

1.4.2 BACK-PANEL FUNCTIONS

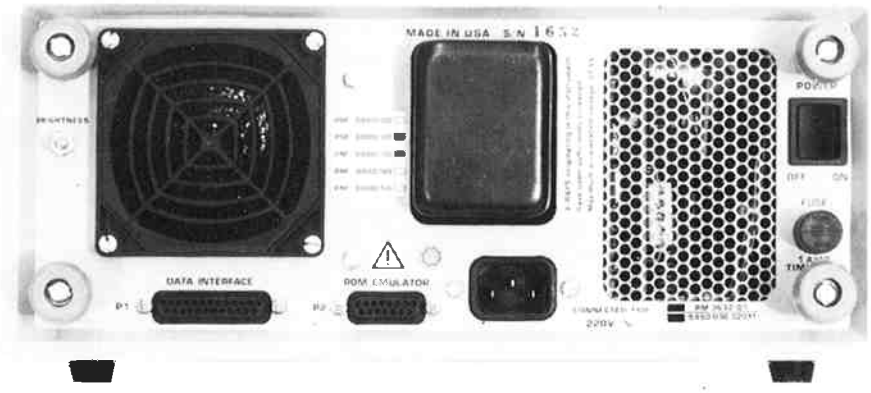


Fig. 1.2 *PM 3632 Back Panel*

From left to right:

BRIGHTNESS ADJUSTMENT
Screwdriver control (with locking nut) for display intensity.

DATA INTERFACE CONNECTOR
RS-232C connection used for data uploading/downloading from a host computer with the:

Rom Emulator Module	PM 8880/00
Set-up Memory	PM 8880/40
Set-up/Data Memory	PM 8880/50

ROM EMULATOR CONNECTOR
15-pin connector to connect the ROM Emulator Pod PM 8864

POWER SWITCH (ON/OFF)

MAINS FUSE: 110-127V : 2 Amps (delayed)
200-250V : 1 Amps (delayed)
5x20mm, glass tube

1.5 AUDIBLE WARNINGS

-ONE BEEP
Warns that a wrong key has been depressed (including trying to move the cursor past the limits of the field or screen), and ignored by the system. For example, depressing a numerical key on a display screen will usually produce one beep.

Upon power-up, one beep verifies that the power is on.

-TWO BEEPS
Signal that data has stopped being recorded, i.e., that the trigger condition has occurred and that the trigger delay has been satisfied.

-THREE BEEPS
Warn that set-up entries are inconsistent, or that there are pod status errors. The screen will display an explanatory error message, such as:
-"ALREADY STARTED" if the START key is depressed during data recording,
-"POD CONNECTION ERROR" if the connection to the unit under test is wrong,
-"NO DATA RECORDED" if the STOP key is depressed before any data has been recorded, etc.

-CONTINUOUS BEEPS
Indicate that a wrong key is being depressed continuously and is repeating.

2. CONNECTION TO THE SYSTEM UNDER TEST

2.1 GENERAL

Signals from the system under test are always applied to the Analyzer via a Pod.
Note that the analyzer configuration is automatically set according to the connected Pod.

Input Pods

The Input Pods contain the necessary circuitry to adapt the signals of the system under test.
For detailed information on these Pods refer to chapter 5.

Four main Pod-versions are available:

-A 32-channel Logic Pod.
 This Pod is provided with separate probe input wires, and can be used for observation of, not only the microprocessor activity, but also for the signals in the asociated circuits.

-A 4-channel 'FAST' Pod. This Pod features 100 MHz sampling, and selectable Glitch- or Non-glitch detection.

-Micro-processor Pods. Various types are available corresponding to the most common micro-processors. These Pods are provided with a micro-processor test clip.

-A Standard Bus Pod. This Pod features direct connection to a Standard Bus system backpanel.

Rom Emulator Pod

This Pod is used for emulation of the Rom Memory of the system under test.
For detailed information refer to chapter 6.

CONNECTION

To connect a Pod to the system under test:
-Switch-off the mains voltage of the Analyzer.
-Insert the Pod cable to the connector at the front panel of the Analyzer.
-Connect the Pod probes or the microprocessorclip to the system under test.
-Switch-on the Analyzer.

WARNING : DO NOT PLUG OR UNPLUG THE POD CONNECTOR, WHILE THE ANALYZER IS POWERED UP.

2.2 32-CHANNEL LOGIC POD

The 32-channel Pod has 42 probes (16 on one probe set and 26 on the other probe set). Each probe input and ground is provided with an EZ hook clip.

The probe set with 16 wires is called the 8-Channel Probe Set ; it contains Probes 0...7, the Clock Probe, the Clock Qualifier Probe and six grounds. This group is equipped for high-speed recording.

The probe set with 26 wires is called the 24-Channel Probe Set, and contains Probes 8-31 and two grounds.

Each probe has 3 parts : the tip (body) and the cap (plunger) of the EZ hook clip, and the wire; each part may be one of 10 colors.

Color coding:
-Clock Probes have all three parts colored red.
-Clock Qualifier Probes are all blue.
-Ground Probes are all black
-The remaining probes all have grey caps.
Refer also to the Color Coding list on the next page.

THRESHOLD VOLTAGE

The Pod contains a switch for selecting either "TTL" or "Variable" voltage threshold.
The "TTL" position sets the TTL level threshold voltage (1.4 V).
The "Variable" position allows setting the threshold voltage between -9 V and +9 V by adjusting the potentiometer located next to the switch.

The threshold voltage can be measured at pin 19 on the pod's 20-pin connector, by using a high-impedance meter. The impedance of this node is about 1 Kohm. Pins 17, 18 or 20 can be used as measuring ground.
Refer to Fig. 2.1.

SET UP

Connect the desired number of probes (corresponding to the number of selected input channels) to the points on the circuit to be tested.

To sample data synchronously (external clock), connect the probe for the clock to the system under test.

The circuits of the input buffers for Clock, Clock Qualifier and Data channels 0--3 have been designed to be very fast, and care must be taken to minimize coupled noise.

WARNING

THE CLOCK AND CLOCK QUALIFIER WIRES SHOULD ALWAYS BE TWISTED WITH A CONNECTED GROUND LEAD. FOR OPERATION ABOVE 10 MHz, THE LOWER DATA CHANNELS SHOULD ALSO BE TWISTED WITH THE GROUND LEADS PROVIDED.

PROBE SET COLOR CODING

8-Channel probe set

Signal	Body (tip)	Plunger (cap)	Wire	Pod Connector Pin
Probe 0	Black	Grey	Black	2
Probe 1	Black	Grey	Brown	3
Probe 2	Black	Grey	Red	5
Probe 3	Black	Grey	Orange	6
Probe 4	Black	Grey	Yellow	8
Probe 5	Black	Grey	Green	9
Probe 6	Black	Grey	Blue	11
Probe 7	Black	Grey	Violet	12
Clock	Red	Red	Red	16
Qualifier	Blue	Blue	Blue	14
Grounds	Black	Black	Black	1/4/7/10/13/15
Threshold	-	-	-	19
Ground	-	-	-	20

24-Channel probe set

Signal	Body (tip)	Plunger (cap)	Wire	Pod Connector Pin
Probe 8	Black	Grey	Grey	2
Probe 9	Black	Grey	White	3
Probe 10	Brown	Grey	Black	4
Probe 11	Brown	Grey	Brown	5
Probe 12	Brown	Grey	Red	6
Probe 13	Brown	Grey	Orange	7
Probe 14	Brown	Grey	Yellow	8
Probe 15	Brown	Grey	Green	9
Probe 16	Brown	Grey	Blue	10
Probe 17	Brown	Grey	Violet	11
Probe 18	Brown	Grey	Grey	12
Probe 19	Brown	Grey	White	13
Probe 20	Red	Grey	Black	15
Probe 21	Red	Grey	Brown	16
Probe 22	Red	Grey	Red	17
Probe 23	Red	Grey	Orange	18
Probe 24	Red	Grey	Yellow	19
Probe 25	Red	Grey	Green	20
Probe 26	Red	Grey	Blue	21
Probe 27	Red	Grey	Violet	22
Probe 28	Red	Grey	Grey	23
Probe 29	Red	Grey	White	24
Probe 30	Orange	Grey	Black	25
Probe 31	Orange	Grey	Brown	26
Grounds	Black	Black	Black	1/14

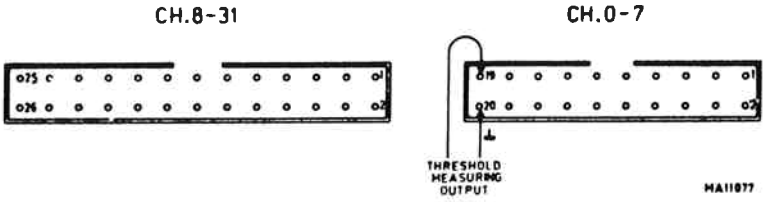


Fig. 2.1 *Connector pin numbering on the 32-channel Pod (as seen on the Pod)*

2.3 4-CHANNEL FAST POD

WARNING : DO NOT PLUG OR UNPLUG THE POD CONNECTOR, WHILE THE ANALYZER IS POWERED UP.

This Pod has 6 twisted wire input pairs terminated in EZ Hook clips. Each signal lead has a resistor in the lead adjacent to the clip, to reduce signal reflection.

INPUT COLOR CODING

	EZ Hooks	
Signal	Body(tip)	Plunger(cap)
Channel 0	Grey	Black
Channel 1	Grey	Brown
Channel 2	Grey	Red
Channel 3	Grey	Orange
External clock	Red	Red
Qualifier	Blue	Blue
Grounds	Black	Black

THRESHOLD VOLTAGE

This Pod contains a switch to select either "TTL" or "Variable" voltage threshold.
The "TTL" position (switch away from the screwdriver slot) sets the TTL level threshold voltage (1.4 V).
The "Variable" position (switch towards the screwdriver slot) allows setting the threshold voltage between -7.9 V and +7.9 V by adjusting the potentiometer located next to the switch.
Provision is made for measuring the threshold voltage by a pair of wires on the probe set which terminates in a 2-pole connector. The threshold voltage may be measured here with the contact on the flat end of the connector being at ground.
Use a high-impedance meter; the impedance of this node is about 1 kohm.

SET UP

To sample data synchronuously with an external clock, connect probes for the clock and (optionally) the clock qualifier to the circuit. The input buffers for Clock, Clock Qualifier, and Data channels 0-3 have been designed to be very fast, and care must be taken to minimize coupled noise.

NOTE : THE CLOCK AND CLOCK QUALIFIER WIRES SHOULD ALWAYS BE TWISTED WITH A CONNECTED GROUND LEAD. FOR OPERATION ABOVE 10 MHz, THE LOWER DATA CHANNELS SHOULD ALSO BE TWISTED WITH THE GROUND LEADS PROVIDED.

THE ALL BLACK EZ HOOKS ARE THE GROUND CLIPS, AND SHOULD BE CONNECTED TO A CIRCUIT GROUND CLOSE TO THE SIGNAL BEING OBSERVED.

THIS POD CONTAINS SEVERAL HIGH-SPEED INTEGRATED CIRCUITS, WHICH DISSIPATE A LARGE AMOUNT OF HEAT. DO NOT USE IT IN ANY POSITION WHICH OBSTRUCTS THE NORMAL AIRFLOW AROUND IT.

2.4 MICRO-PROCESSOR PODS

WARNING : DO NOT PLUG OR UNPLUG THE POD CONNECTOR, WHILE THE ANALYZER IS POWERED UP.

To connect a micro-processor Pod, insert its cable connector plug into the connector on the front panel, then clip the probe to the micro-processor.
The brown wire on the colored ribbon cable must connect to Pin 1 of the micro-processor (this must correspond with the '1' indication on the Pod near the connector of the microprocessor clip ribbon cable).
Information obtained internally from this Pod will determine some of the PM 3632 set-up parameters.

Refer to chapters 5.4 and 5.5.

2.5 STANDARD BUS POD

WARNING : DO NOT PLUG OR UNPLUG THE POD CONNECTOR, WHILE THE ANALYZER IS POWERED UP.

The STANDARD Bus Pod consists of a p.c. extender board and a cable for connection to the PM 3632.

To connect the STANDARD Bus Pod, attach its cable connector plug to the connector on the front panel. Insert the circuit card into an unused slot in the STANDARD bus backplane of the unit under test, or install it as an extender between the bus and a card on the bus.
For detailed information refer to chapter 5.

2.6 ROM EMULATOR POD

WARNING : DO NOT PLUG OR UNPLUG THE CONNECTOR, WHILE THE ANALYZER IS POWERED UP.

To connect the ROM Emulator Pod, insert the module's connector into the ROM EMULATOR connector receptacle on the back panel. Then plug the proper DIL plug directly into the ROM sockets of the system under test.
For detailed information refer to chapter 6.

3. SET-UP SCREENS (MENUS)

3.1 GENERAL

To set up the PM 3632 for operation, use the front-panel set-up keys : CLOCK, CONFIG, TRIG, SEQ, DELAY and FORMAT.
Each of these keys calls up a CRT screen offering parameter selections and/or set-up information. Changeable fields on the CRT display are reverse-videoed and the cursor position blinks; the cursor automatically skips over non-changeable fields.
The STATUS key selects the STATUS display which contains the main status parameters. There are no changeable fields in this display.

Each screen contains complete prompting information about how to set-up each parameter, including exactly what the preset options are, the specific key designated to select each option, and the allowable ranges of parameter values.
Also, the system protects against most wrong entries and selections, by not accepting them, and beeping to warn the user.

As soon as a parameter has been set, any other parameter dependent upon it is updated and displayed, usually immediately. In some cases, a dependent parameter is not updated until the cursor has left the field of the parameter being changed.

To select or change any set-up or display parameter, simply move the cursor to the parameter's field, which will cause it to blink, indicating its readiness to be set up.

Each parameter may be set in one of two ways:
-A limited number (usually 2 or 3) of preset options, entered via the function keys f1--f4.
-The actual value of a parameter (usually numeric) entered via the hexa-decimal keys (0--F), including the "X" (don't care)- and the CLEAR key.

While the PM 3632 is recording, a blinking "ACTIVE" message is displayed in the upper right of the six set-up screens ; during this time, set-up parameters may be viewed on each screen, but not changed.

Note:
To change a parameter on any set-up screen, recording must first be stopped (by depressing "STOP").

3.2 SYSTEM STATUS SET-UP SCREEN

To view overall major system parameters, depress the STATUS key on the front panel.

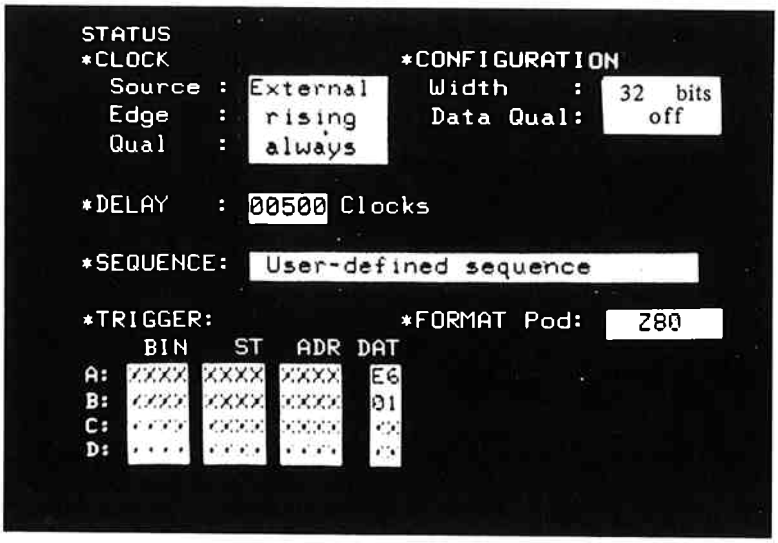


Fig. 3.1 *System Status set-up screen after power-on.*

To view system parameters in greater detail than is shown on the System Status set-up screen, to set up the PM 3632 for initial operation, and/or to change any detailed system parameters while using the PM 3632, use the the following set-up keys on the front panel :

CLOCK	(Recording/sampling rate and clock qualification)
CONFIG (Configuration)	(Recording width/number of channels and data qualification)
TRIG (Trigger) SEQ (Trigger Sequence) DELAY (Trigger Delay)	(Triggering condition, which stops the recording process)
FORMAT (or use default format)	(Data display format)

Refer to Figure 3.1 System Status Set-up Screen, as an example of how one particular set of selections will be displayed.

NOTE :
Labels which are preceded by asterisks refer to keys which access those parameters.

Following are the system parameters as they are displayed on the System Status screen and the selections for each parameter which are available to the user.

CLOCK

```
          Source : Internal
          Period : .... nsec   (4-digit numerical value and units)

   or,    Source : External
          Sense  :  rising  or falling (Edge)
          Qual   : Always, Low or High (Clock qualification)
```

CONFIGURATION

```
          Width     : 32, 16, 8 or 4 bits
          Data Qual : Off

   or,

          Width     : 32, 16, 8 or 4 bits
          Data Qual : Comb.
          Record    : Only or All but

          Occur. of : None or ..... (Trigger words)

   or,

          Width     : 32, 16, 8 or 4 bits
          Data Qual : State
          Enable    : None or ..... (Trigger words)
          Disable   : None or ..... (Trigger words)
```

TRIGGER DELAY

```
          *DELAY    : ..... Clocks (5-digit value; default =00000)
```

TRIGGER *SEQUENCE : .....

Displays the sequence from the 19 possible sequences as shown in the Trigger Sequence screen see Figure 3.5.

*TRIGGER:

```
    A: ......
    B: ......
    C: ......
    D: ......
```

Displays the selected trigger words in number base and the selected or default (List) display format. Default is all "Xs".

*FORMAT Pod: ..... (mode)

Most pods have more than one mode, in which case the f1, f2, f3 or f4 key is used to select the particular mode via the Display Format set-up screen: e.g., the f1 key would select the 8085 mode of the PM 8865 micro-processor pod.

3.3 CLOCK SET-UP SCREEN

To call up the Clock set-up screen, depress the CLOCK key. This screen displays the internal and external clocking parameters and is used to select and change specific parameters.

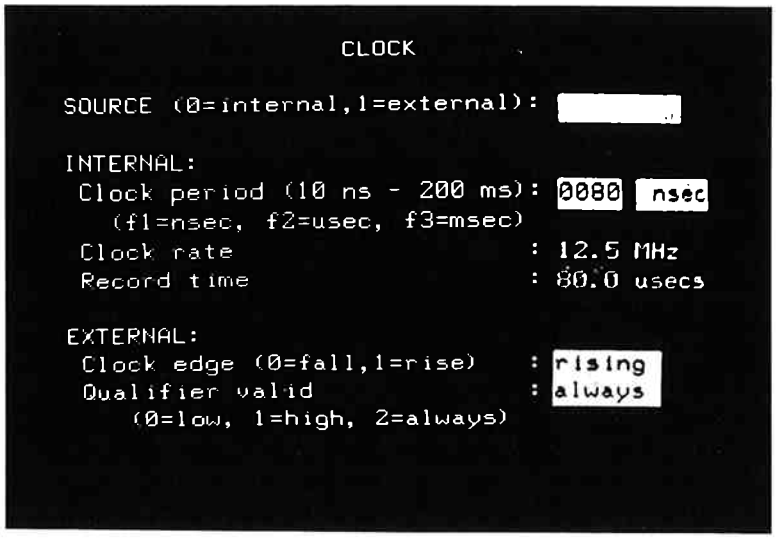


Fig. 3.2 *Clock Set-up Screen after Power-up*

SELECTING THE CLOCK SOURCE

The internal clock (generated by the Analyzer itself) is used when analyzing problems related to logic, hardware and timing, and when measuring time. (Asynchronous clock).
Generally the internal clock is set to a frequency much higher than the clock of the system under test.

The external clock (taken from the system under test) is used for analyzing bus problems ,software and occurences synchronous to the system under test. (Synchronous clock).

External clock rates may not exceed 70 MHz (4-bit mode). For rate limits in other modes, refer to chapter 1.3 'System Specificatons'.

To select (clock) Source, move the cursor to the field labeled "Source", then select either "Internal" by depressing the 0 key on the keypad, or "External" by depressing the 1 key on the keypad.
The internal clock uses time periods in nanoseconds (nsec), microseconds (usec), or milliseconds (msec).

USING THE INTERNAL CLOCK

To set the clock period (from 10 nsec to 200 msec), move the cursor to the first field to the right of "Clock period" and enter the desired value via the hexadecimal keypad. Then move the cursor to the second field and press one of the three preset options for units by depressing f1, f2, or f3.
The corresponding clock (recording) rate, or frequency, and record time will be automatically displayed as soon as the cursor leaves the Clock Period numerical field.

Not every frequency is available. When an unavailable selection is made, the closest available clock frequency will be automatically selected.

USING AN EXTERNAL CLOCK

The external clock is generally taken from the system under test.
The clock detection circuitry of both the PM 8860 and the PM 8862 is very high speed.
To avoid extra clocks due to stray pickup, a connected ground lead should always be twisted with the clock lead. The PM 8862 leads are twisted pairs, but the PM 8860 leads are not.
Failure to twist a connected ground lead with the clock lead is likely to produce extra ("double") clocking; if these clocks occur at a period of less than the minimum, the Analyzer may function incorrectly.

NOTE :
Because of the PM 3632's internal configuration, a minimum of 17 clocks must occur after the trigger condition for correct operation. These 17 clocks are automatically accounted for in all displays ; the user need not be concerned about them unless the external clock stops within 17 clocks of the trigger event.

Clock Edge

To select the Clock Edge (the edge of the clock at which data is to be sampled), depress the 0 key for "Falling" or the 1 key for "Rising". "Falling" means that the data is sampled on the high-voltage-to-low-voltage transition of the external clock input, as it crosses the threshold voltage ; "Rising" means that data is sampled on the upward transition.

Clock Qualifier

To select the clock qualifier, depress 0 (Low), 1 (High), or 2 (Always) on the keypad. "Low" means that the qualifier is valid only when the qualifier input is low ; and "Always" means that the qualifier is always valid (don't care). External clocks are recognized only when the qualifier is valid.

NOTE:
The clock qualifier has no effect with the internal clock.

3.4 CONFIGURATION SET-UP SCREEN

To call up the Configuration set-up screen, depress the CONFIG key.

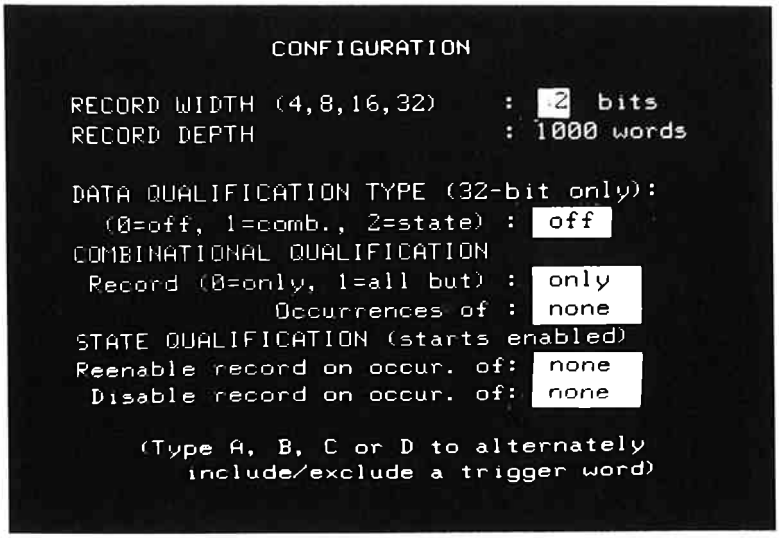


Fig. 3.3 *Configuration Set-up Screen*

This screen shows information about the Record Width related to the Record Depth, and the Data Qualification parameters.

RECORD WIDTH

To select the Record Width, move the cursor to the field labelled "Record Width" and enter the number of bits (channels) (4, 8, 16, or 32), on the keypad. If any other value is entered, it will not be accepted, and the next highest of these four values will be displayed.

The record depth (available memory) will then be automatically displayed. A higher number of channels has less record depth ; e.g., 8000 samples per channel will be recorded in the 4-channel mode, and 1000 samples per channel in the 32-bit mode).

The maximum clock rate (speed) for each record width varies from 100 MHz (for 4-bit) to 12.5 MHz (for 32-bit).

The following tabel shows the relationships between record width, clock rate (speed), and record depth.

Record width	Max. clock freq.	Record depth
4 bits (int. clock)	100 MHz	8000 samples/words
4 bits (ext. clock)	70 MHz	8000 samples/words
8 bits	50 MHz	4000 samples/words
16 bits	25 MHz	2000 samples/words
32 bits	12.5 MHz	1000 samples/words

DATA QUALIFICATION (in the 32-bit mode only)

Data qualification is used to record only desired pieces of data (blocks), to conserve memory, and to make problem areas more visible. It permits determination on an individual (combinational) or sequential (list) basis as to whether or not any given word (data sample) will be recorded. It is available in 32-channel mode only.
Note that data qualification does not affect recognition of trigger words, but does affect the trigger delay ; i.e., a word included in the trigger sequence will be recognized regardless of whether or not data qualification allows it to be recorded, but only qualified words are counted in the trigger delay.

To select the type of Data Qualification, enter a 0 (Off), a 1 (Combinational), or a 2 (State) via the keypad.

To select the trigger words to be used as data qualifiers, use the A...D keys. When more than one word is entered, the display will automatically show a "+" between the words, meaning "or". Each A...D key toggles on/off when depressed repeatedly, causing the character to alternately appear and disappear.

Combinational Data Qualification

To select a combinational data qualifier, depress 0 (only) or 1 (All but) in the field labeled "Record", then enter A, B, C and/or D in the "Occurrence of" field to indicate the trigger words upon which the selected qualifier will act. All four trigger words (A...D) may be used. Setting of trigger words is described in chapter 3.5.

For example, to record only program fetches in the area of 0100H to 02FFH when using a micro-processor pod, proceed as follows:
-Set the trigger Word C to fetches with the Address field 01XX and the Data field XX.
-Set the trigger word similarly, with 02XX in the Address field.
-Set Data Qualification Type to "Comb"
-Set "Record" under Combinational Qualification to "only"
-Set "Occurences of" to "C+D".

State Data Qualification

To select a state data qualifier, enter the selected trigger conditions upon which recording will be enabled or disabled in the appropriate fields Recording always begins when the START key is depressed.

Only one or two trigger words per field may be used ; although the field is large enough to enter three or four words, the logic analyzer will not start recording data if more than two have been entered.

NOTE :
When state data qualification is being used, trigger word "D" is not available for trigger sequence and, if either field ("Reenable .." or "Disable ..") contains two words, then trigger word "C" is also unavailable for trigger sequence. (It is convenient to use "C+D" for data qualification, so as to leave A and B open for triggering).
For example, with state qualification, to record everything from the time an instruction is fetched at 3F27H until an instruction is fetched at 4010H, set trigger words C and D to fetches at those locations, enable state qualification, and set "Reenable .." to C and "Disable .." to D.

3.5 TRIGGER SET-UP SCREEN

The TRIG key calls up the Trigger set-up screen with which four trigger words (events), labeled "A", "B", "C", and "D", are displayed and defined.

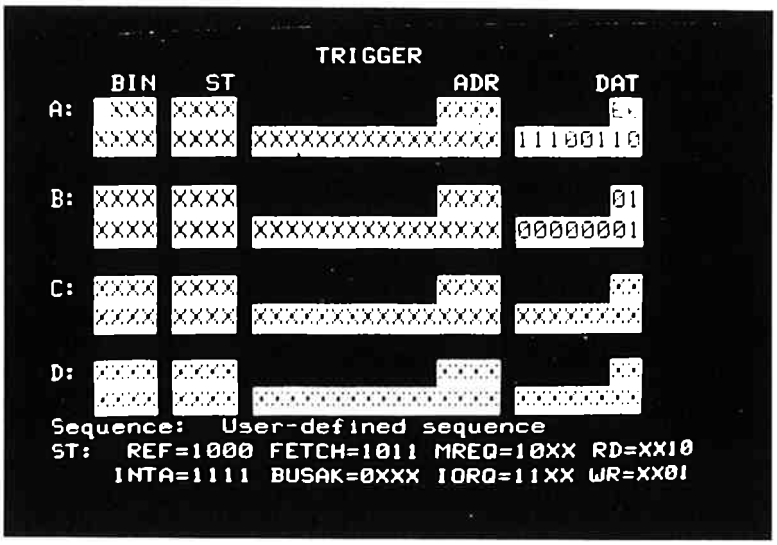


Fig. 3.4 *Trigger Set-up Screen*

On the display, there are two lines per trigger word.
The first line shows the trigger word in the number base as selected in the Format screen (not in ASCII).
The second line always shows the trigger word in binary.
There is no separate field for the trigger format.

Fields are displayed from left to right, in ascending numerical order ; "off" fields are not displayed. All numbers are displayed with the least sufficient digit at the right of the field ; for binary fields, this means Bit 0 is at the right of the field.

To define a trigger word, move the cursor to either (first or second) line and use the keypad to enter the appropriate value.
The value on the other line will be changed accordingly.
To change any character in a trigger word, just move the cursor to the appropriate position, and enter the character via the keypad.

With the 32-ch. logic pod, the default number base for the upper line is binary, and is so labeled on the screen.
With micro-processor and bus pods, the default number base is hex for many fields, but is determined by the particular pod and its requirements.
Micro-processor pods also label fields as "STS" (status bits), "ADR" (address), and "DAT" (data).

An attempt to enter a value which is too large for the selected number base will be rejected, and will cause the unit to beep once as an error warning.

In decimal number base, as further protection against entering unacceptable values, the PM 3632 will truncate the upper bits of a value that is larger than allowed : e.g. in decimal number base, if "18" is entered in a 4-bit field, as soon as the cursor leaves the field, the "18" is truncated to "2", an acceptable value).

To change the number base from the default or previously set base, use the Display Format screen via the FORMAT key. Refer to Chapter 3.8.

To indicate a "Don't Care" when entering a trigger word on either line, depress "X" on the keypad. Any resulting indeterminate character on the upper line will be displayed as a "?". In decimal number base, a "Don't Care" may not be entered for an individual digit because of the binary nature of the unit.

The bottom two lines of this set-up screen may contain information about the status fields. The presence of such information depends upon which micro-processor pod is being used and whether the appropriate disassembler has been installed in the PM 3632.
Possible status code prompts are :

FETCH	Instruction fetch (first byte of an instruction)
MRD	Memory read
MWR	Memory write
HLDA	Hold acknowledge
INTA	Interrupt acknowledgement
IORD	I/O read
IOWR	I/O write

See chapter 5.4, Micro-processor Pods, for further details of the status codes.

Figure 3.4 shows four trigger words defined to be matched with any type of access (fetch, read, write, etc.) to one of four addresses.
In all four cases shown, the trigger condition is satisfied no matter what data is transferred during that cycle (Data is don't cares).

3.6 TRIGGER SEQUENCE SET-UP SCREEN

The Trigger sequence screen is shown after pressing the SEQ key.
The trigger sequence defines the trigger condition which will stop the recording of data after the selected trigger delay.
If the delay is zero, recording stops immediately upon occurrence of the trigger condition.

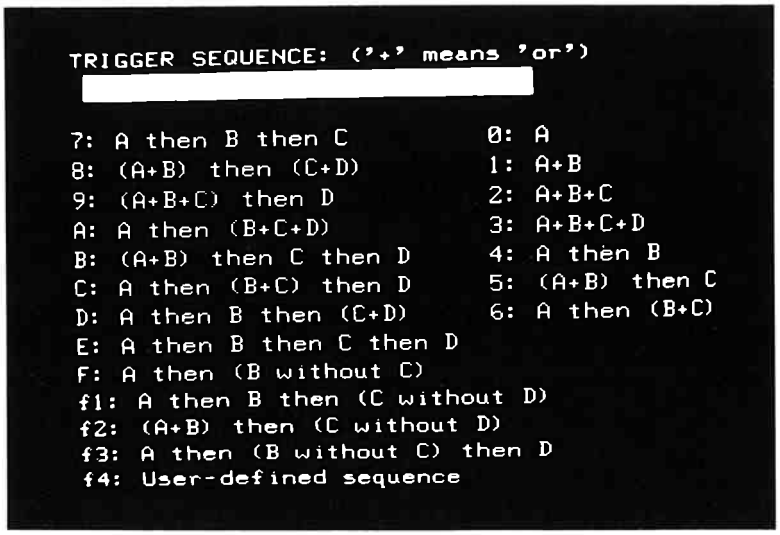


Fig. 3.5 *Trigger Sequence Set-up Screen*

A trigger sequence condition is formed by various combinations or sequences of the selected trigger words (events), up to four words (labeled A, B, C and D) and four levels. Trigger words are defined via the Trigger set-up screen. Refer to chapter 3.5.

The Trigger Sequence set-up screen is used to select (and to change the selection of) any of the pre-defined trigger sequences, and to access (via the f4 key) the User-Defined Sequence set-up screen.

PRE-DEFINED TRIGGER SEQUENCES

The Trigger sequence screen is shown after pressing of the TRIG key.
This screen displays the 19 pre-defined trigger sequences, which are listed in Figure 3.5, along with the corresponding keypad entries for selecting them.

To select a pre-defined trigger sequence, depress the key which corresponds to the selected sequence; it will then be displayed on the second line of the screen, and may be changed via the keypad.
"0" (predefined as "A") is the default setting.

Other selections include combinations or sequences of trigger words (events) to make up the trigger condition. E.g., the sequence designated "7" ("A then B then C") will cause recording to continue until trigger word "A" is encountered, then until trigger word "B" is encountered, then until triggerword "C" is encountered. At this point, the entire trigger condition has been satisfied, and the delay will begin. Recording will stop immediately if the delay is zero.

Sequence f1 ("A then B then (C without D)") is identical to Sequence 7, except that, if "D" is encountered after "B" but before "C", then the PM 3632 will begin again to search for "A".

This sequence can be very useful when it is desired to trigger only when one event occurs immediately after another. To do this, use a sequence such as the f1 sequence, with "D" containing all "Don't Cares" : in this case, "B" and "C" will have to occur with no other cycles in between to satisfy the trigger condition.

Only in the 32-channel operation are all 19 trigger sequences (including the user-defined sequence) available, as shown in the table below.

Record width	Available Trigger sequences
4 channels	0, 1, 2, and 3
8 channels	0, 1, 2, and 3
16 channels	0, 1, and 4
32 channels	All (including user-defined)

USER-DEFINED TRIGGER SEQUENCE

To select or change the user-defined trigger sequence, first depress the f4 key, which brings up a new screen ("User-Defined Sequence") and presents a complex sequence format with one to four levels.

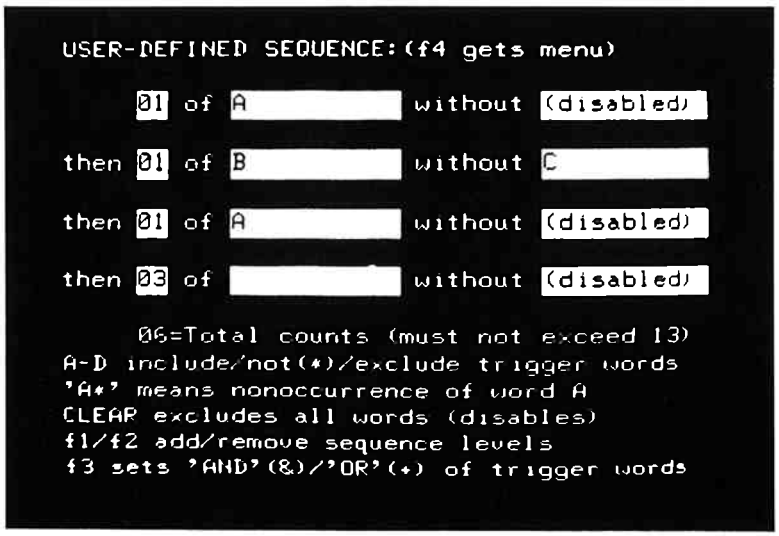


Fig. 3.6 *User-defined Sequence Set-up Screen*

Each level displays three fields: a 2-digit field for number of counts for that level, an 11-character field for a trigger word combination, and a second 11-character field for a "without" trigger word combination.
When recording, the PM 3632 waits at each level until that condition has been satisfied.
If the entered count for a level is greater than one, then that level must be satisfied that number of times before the PM 3632 proceeds to the next level. If the "without" condition is encountered at a level, then the whole sequence starts over at the first level.

The screen's default format displays only the first trigger sequence level. To add a level, depress the f1 key; to remove the lowest level, depress the f2 key.

To enter the number of counts for each level, enter the value via the keypad. Up to 13 total counts (among all four levels) are allowed; e.g., if a total of 9 counts has been entered into the first three levels, then no more than 4 counts may be entered into the fourth level. After entry of the number of counts for a level, the new total number of counts is displayed as soon as the cursor is moved. Any level whose count is greater than 13 will be limited to 13 if its count field is exited. If the new total number of counts exceeds 13, any attempt to leave the screen vauses the PM 3632 to beep 3 times, flashes the "must not exceed 13" message, and does not allow leaving the screen.

To enter the trigger word combinations for each level, use the keypad to enter the desired combination of available trigger words ("A", "B", "C", and "D").
To include a trigger word, depress the key quickly and surely, do not linger on the key or it will repeat and change the entry.

If a word has already been entered in the field, the new word will be entered as an "or" word (shown as "+") or as an "and" word (shown as "&"), depending upon the mode. E.g., in the "or" mode, if "A" is already in the field, depressing the B key will enter "+B", and the field will show "A+B", meaning "A or B".

To change an entered trigger word to a "not" condition, depress the same key a second time (with the cursor in the appropriate field), and the display will place a "*" ("not").
E.g., if "A+B" is already in the field, depressing the B key will add an asterisk to the "B", and the field will show "A+B*", meaning "A or not B".

To exclude an entered trigger word, depress the same key a third time and the word (and its attached asterisk) will disappear from the field display. If the word was not a negative, i.e., had no asterisk, the key must be depressed twice toggling through the negative condition to get to the excluded one.

Depressing the same key a fourth time will toggle back to include the trigger word, etc., repeating the pattern of inclusion/negation/exclusion endlessly.

To change (all of) the "+" ("or") characters in the trigger word to "&" ("and"), depress the f3 key ; depressing f3 again toggles all the "&" characters back to "+" characters, in another repeating pattern.

To exclude (erase) an entire trigger word sequence from a field, depress CLEAR, and the display will show "(disabled)" is the field.

To return to the Trigger Sequence set-up screen, depress the f4 key, which toggles the display back and forth between the Trigger Sequence and the User-Defined Sequence set-up screens.

NOTE :
When setting a user-defined sequence, be sure to exit from the User-Defined Sequence set-up screen directly to any screen <u>except</u> the Trigger Sequence set-up screen. Exiting from the User-Defined Sequence set-up screen directly to the Trigger Sequence set-up screen will reset the Trigger Sequence to its default condition (Sequence 0, which is "A") ; the user-defined sequence will be remembered, but will not be used to trigger the analyzer.

To collect data without the possibility of a trigger condition stopping the recording of data (i.e., to collect data indefinitely until the STOP key is depressed), set the user-defined trigger sequence to exclude all trigger words by entering "01" as the number of counts, then depressing CLEAR to enter "disabled" in both trigger word fields. The display will then show "0 of (disabled) without (disabled)". This works only in the 32-channel mode.

NOTE :
Entering a number in the second field is only an alternate means of setting the trigger delay (the delay from the trigger event until stopping of the recording process). Trigger delay forces a number of data words to be stored after the trigger event. It cannot, however, guarantee the number of words before the trigger event.

For example, if the trigger condition is satisfied on the tenth clock, there will be only ten data words prior to the trigger.
Sometimes this makes it difficult to capture the beginning of a software loop. This can be overcome by triggering on a second occurrence of a particular event.
For example, trigger word "A+B" could be set to the same thing and a sequence of "A then B" set into the machine.
Alternatively, a user-defined sequence of 13 occurrences of A would cause a minimum of 12 full copies of the loop in memory prior to the trigger event.

3.7 TRIGGER DELAY SET-UP SCREEN

The Trigger Delay set-up screen is shown after pressing the DELAY key.

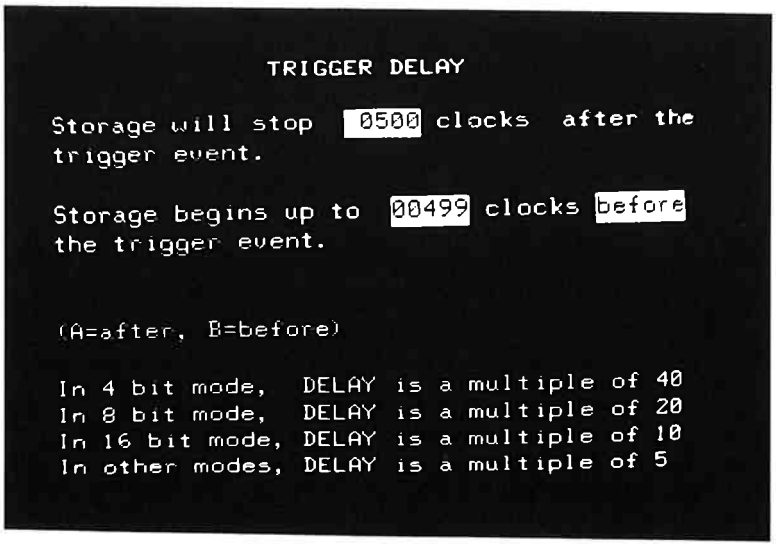


Fig. 3.7 *Trigger Delay Set-up Screen*

To delay the stopping of recording ("storage") of data past the occurence of the trigger condition, a number of samples can be defined before the data recording really stops.
Use the keypad to enter (in the top field) the number of qualified clocks after the trigger condition occurrence at which recording (storage) should stop. This top-field value is the "trigger delay".

Or, to begin recording at a selected number of clocks after of before the trigger condition occurrence, enter that number of clocks in the second field, then select "A" (after) or "B" (before) in the third field.
A sufficiently long trigger delay will place the entire recording interval after the trigger condition.

Only one of the two clock-number fields need to be entered ; the corresponding number in the other number field will be automatically displayed. The distance between these two numbers is the record depth.
The delay period includes only clock-qualified and data-qualified clocks.

NOTE :
The number of samples as trigger delay can be set on values lower than 17. Because the PM 3632's internal configuration, a minimum of 17 clocks must occur after the trigger condition for correct operation. These 17 clocks are automatically accounted for in all displays ; the user need not be concerned about them unless the external clock stops within 17 clocks of the trigger event.

4.3 LIST DISPLAY

4.3.1 INTRODUCTION

The List Display is shown after pressing the LIST key.

Two main list displays are possible:
-The Logic (or Fast) Pod List display (fig. 4.2)
-The Micro-processor List display (fig. 4.3).

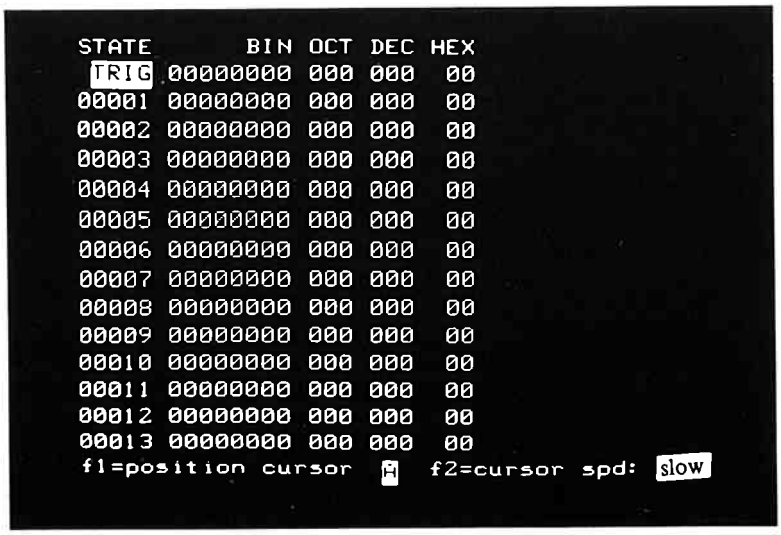


Fig. 4.2 *Logic Pod List Display (LOGIC 32)*

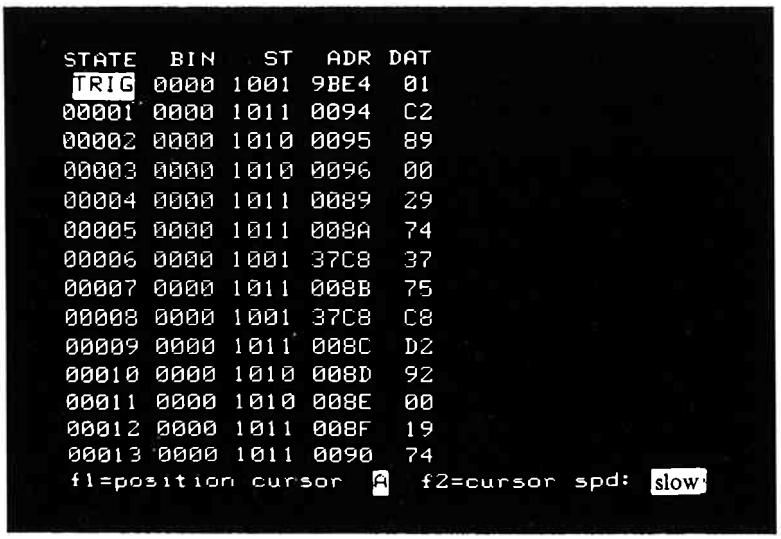


Fig. 4.3 *Microprocessor Pod List Display (8085)*

Each line of this screen represents one data sample, displayed in bit groupings and number base as selected in the Display Format screen.
The trigger condition (or the first data-qualified word in storage which follows the trigger condition), if present in memory, is labelled "TRIG".

To display the trigger condition, scroll up or down via the arrow keys, or move directly to the Triggerword by pressing the LIST key a second time.

To scroll up or down through the data samples, use the arrow keys.

4.3.2 MEMORY A or B?

When the PM 3632 has been provided with an optional Setup/Data-Memory (PM 8880/50), selection can be made to display the A or the B memory.
The A or B is shown on the bottom line on the display.
Selection is executed by pressing the A or the B key.
Refer to the description of the PM 8880/50 (chapter 6).

4.3.3 LOGIC POD LIST DISPLAY

Figure 4.2 shows an example of a Logic Pod data list display.

STATE column

This column indicates the sequence of the samples.
When the Triggerword is in the acquisition memory, the numbers in this column are related to the Triggerword.
When the Triggerword is not in the acquisition memory, these numbers represent the acquisition memory addresses.

DATA Columns (BIN, OCT, DEC, HEX or ASC)

These columns show the input signals. The display format, as well as the number-base is as selected in the FORMAT display.
Each column is displayed with the l.s. digit at the right-hand side.

4.3.4 MICROPROCESSOR POD LIST DISPLAY

Figure 4.3 shows an example of a Microprocessor Pod data list display.

BIN column

This column represents the signals as connected to the side-inputs of the Microprocessor Pod. The number-base of this column can be changed in the FORMAT display.
Refer to the description of the specific Pod (chapter 5).

4.3 LIST DISPLAY

4.3.1 INTRODUCTION

The List Display is shown after pressing the LIST key.

Two main list displays are possible:
-The Logic (or Fast) Pod List display (fig. 4.2)
-The Micro-processor List display (fig. 4.3).

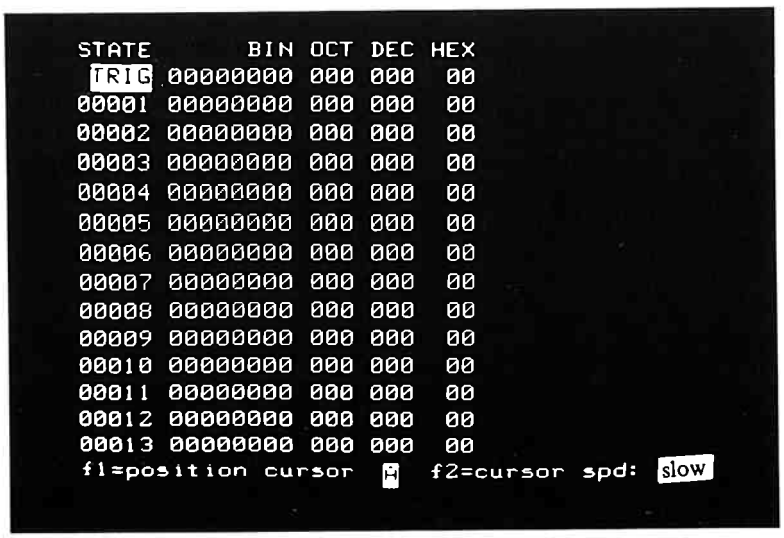


Fig. 4.2 *Logic Pod List Display (LOGIC 32)*

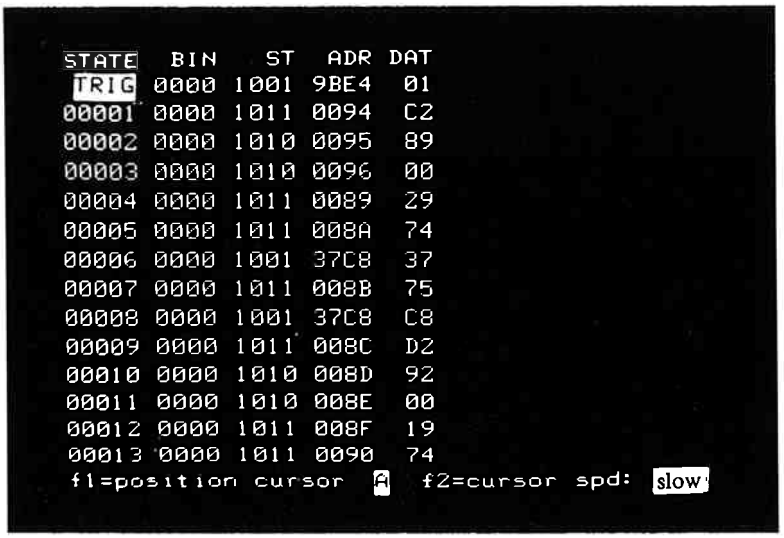


Fig. 4.3 *Microprocessor Pod List Display (8085)*

Each line of this screen represents one data sample, displayed in bit groupings and number base as selected in the Display Format screen.
The trigger condition (or the first data-qualified word in storage which follows the trigger condition), if present in memory, is labelled "TRIG".

To display the trigger condition, scroll up or down via the arrow keys, or move directly to the Triggerword by pressing the LIST key a second time.

To scroll up or down through the data samples, use the arrow keys.

4.3.2 MEMORY A or B?

When the PM 3632 has been provided with an optional Setup/Data-Memory (PM 8880/50), selection can be made to display the A or the B memory.
The A or B is shown on the bottom line on the display.
Selection is executed by pressing the A or the B key.
Refer to the description of the PM 8880/50 (chapter 6).

4.3.3 LOGIC POD LIST DISPLAY

Figure 4.2 shows an example of a Logic Pod data list display.

STATE column

This column indicates the sequence of the samples.
When the Triggerword is in the acquisition memory, the numbers in this column are related to the Triggerword.
When the Triggerword is not in the acquisition memory, these numbers represent the acquisition memory addresses.

DATA Columns (BIN, OCT, DEC, HEX or ASC)

These columns show the input signals. The display format, as well as the number-base is as selected in the FORMAT display.
Each column is displayed with the l.s. digit at the right-hand side.

4.3.4 MICROPROCESSOR POD LIST DISPLAY

Figure 4.3 shows an example of a Microprocessor Pod data list display.

BIN column

This column represents the signals as connected to the side-inputs of the Microprocessor Pod. The number-base of this column can be changed in the FORMAT display.
Refer to the description of the specific Pod (chapter 5).

ST column

This column shows the microprocessor-status, such as instruction-fetch, memory-write, wait-state etc.
For the explanation of the status refer to the description of the specific Pod (chapter 5).

ADR column

This column shows the address related to the microprocessor action.

DAT column

This column shows the data related to the microprocessor action.

4.4 DISASSEMBLY DISPLAY

4.4.1 INTRODUCTION

The Disassembly Display is shown after pressing the DISA key.

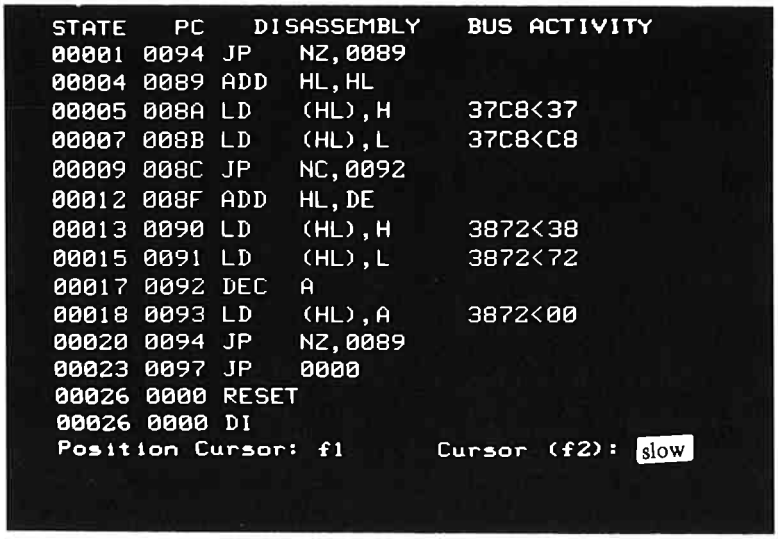


Fig. 4.4 *Disassembly Display Screen*

The Disassembly mode displays data collected via an (optional) micro-processor pod, which enables the PM 3632 to display the recorded data as assembly-language micro-processor instructions ("reverse assembly").

When data qualification is being used, some ambiguities in the recorded data may result.

4.4.2 STATE column

This column shows the State numbers corresponding with the normal LIST display.
Note that not all State numbers are displayed, because each complete microprocessor instruction is displayed on one line.
The TRIG condition is only shown if the word which completes the trigger condition contains the first byte of the instruction.

4.4.3 PC column

This column shows the contents of the microprocessor-programmcounter at the instruction fetch (first byte).

4.4.4 DISASSEMBLY column

This column shows the Mnemonics of the disassembled microprocessor-instructions.
For explanation of the Mnemonics refer to the microprocessor-handbooks.

4.4.5 BUS ACTIVITY column

This column shows the actual data transfers on the microprocessor bus.

E.g. 0800->16 The contents of memory-address 0800(H) = 16
0801<-00 00 is written into memory address 0801(H)

5. *DESCRIPTION OF THE PODS*

5.1 PM 8860 32-CHANNEL LOGIC POD

5.1.1 INPUT PROBES

This Pod has 42 probes (16 on one probe set, and 26 on the other probe set). Each probe input and ground is provided with an EZ hook clip.

The probe set with 16 wires is called the 8-Channel Probe Set; it contains Probes 0...7, the Clock Probe, the Clock Qualifier Probe and six grounds. This group is equipped for high-speed recording.

The probe set with 26 wires is called the 24-Channel Probe Set, and contains Probes 8-31 and two grounds.

Each probe has 3 parts : the tip (body), the cap (plunger) of the EZ hook-clip, and the wire ;
each part may be one of 10 colors.

Color coding:
-Clock Probes have all three parts colored red.
-Clock Qualifier Probes are all blue.
-Ground Probes are all black
-The remaining probes all have grey caps.
Refer also to the Color Coding list in chapter 2.

5.1.2 THRESHOLD VOLTAGE

The Pod contains a potentiometer and a switch for selecting either "TTL" of "Variable" voltage threshold.
The "TTL" position sets the TTL level threshold voltage (1.4 V).
The "Variable" position allows setting the threshold voltage between -9 V and +9 V by adjusting the potentiometer located next to the switch.

The threshold voltage can be measured at pin 19 on the pod's 20-pin connector, by using a high-impedance meter. The impedance of this node is about 1 Kohm. Refer to Figure 2.1 (chapter 2).

5.1.3 SET-UP

Connect the desired number of probes (which corresponds to the number of selected input channels) to the points on the circuit to be tested.

To sample data synchronuously (external clock), connect the probe for the clock to the circuit to be tested.

The circuits of the input buffers for Clock, Clock Qualifier, and Data channels 0-3 have been designed to be very fast, and care must be taken to minimize coupled noise.

WARNING : THE CLOCK AND CLOCK QUALIFIER WIRES SHOULD ALWAYS BE TWISTED WITH A CONNECTED GROUND LEAD. FOR OPERATION ABOVE 10 MHz, THE LOWER DATA CHANNELS SHOULD ALSO BE TWISTED WITH THE GROUND LEADS PROVIDED.

5.2 PM 8862 4-CHANNEL FAST POD

WARNING : THIS POD CONTAINS SEVERAL HIGH-SPEED INTEGRATED CIRCUITS, WHICH DISSIPATE A LARGE AMOUNT OF HEAT. DO NOT USE IT IN ANY POSITION WHICH OBSTRUCTS THE NORMAL AIRFLOW AROUND IT.

5.2.1 INPUT PROBES

The 4-Channel high-speed Pod has six probes : four for data, one for an external clock, and one for clock qualification.
Each probe consists of two EZ hook clips attached to a length of twisted-pair cable.
The all-black hook in each pair is a ground probe, and should be connected to a circuit ground local to the signal being observed.
The remaining six hooks are color coded as follows :

FUNCTION	BODY (tip)	PLUNGER (cap)
Channel 0	Grey	Black
Channel 1	Grey	Brown
Channel 2	Grey	Red
Channel 3	Grey	Orange
External clock	Red	Red
Clock Qualifier	Blue	Blue

5.2.2 THRESHOLD VOLTAGE

Provision is made for measuring threshold voltage by a pair of wires on the probe set which terminates in a Molex connector. The threshold voltage may be measured here with the contact on the flat end of the connector being at ground.

To adjust the threshold voltage, use the switch and potentiometer which are accessible through a slot in the end of the pod. When the switch is towards the screwdriver slot, the potentiometer may be used to vary the threshold over a +/- 7.9 V range. When the switch is away from the screw-driver slot, the threshold is fixed ad 1.4 v for use in TTL-level circuits.

5.2.3 SET-UP

Selection of trigger and clock parameters are made in the same manner as they are for the 32-Channel Logic Pod (PM 8860).

5.2.4 GLITCH CAPTURE

The Glitch mode or the No-Glitch mode can be selected in the Format display.
Glitches are fast pulses which may occur in between two sample clocks.
In the No-Glitch mode these signals are not detected.
In the Glitch Capture mode, if an even number of data transitions occur between successive sample clocks, then the displayed data will alternate during the two clock periods following the one in which the glitch occured.

5.3 PM 8863 STANDARD BUS POD

5.3.1 INTRODUCTION

The STANDARD Bus Pod enables the PM 3632 to capture bus cycles asynchronously (with the internal analyzer clock) or synchronously (with the external clock).
The Pod may be inserted into an unoccupied slot on the bus, or it may be used as an extender card, by plugging the card which normally occupies the bus slot into the STANDARD Bus Pod, then inserting the Pod into the bus slot.

5.3.2 MODES

The Pod has three modes, as shown on the Format set-up screen: STDBUS, STDINT, and STD24B.
The first 24 data lines are the same in each of these modes, the remaining 8 data lines differ among the three modes, and, by altering jumpers on the board, the signals presented in the first two modes can be selected by the user. Data lines for each of the three modes are shown in the table below.

Data lines	STDBUS	STDINT	STD24B(default)
0...7	Data	Data	Data
8..23	Address (lower 16 bits)	Address (lower 16 bits)	Address (lower 16 bits)
24	RD*	INTRO* (see jumper options)	--]
25	WR*	INTAK*	]
26	IORQ*	IORQ*	]
27	MEMRQ*	PCI	]
28	IOEXP (if IORQ* is active) MEMEX (if MEMRQ* active)	PCD	] >Adress] (upper 8 bits)]
29	BUSRQ*	REFRESH*	]
30	BUSAK*	STATUS0*	]
31	WAITRQ*	STATUS1*	]

= Signal names followed by an '' are activ low.

The STDBUS mode, with default jumpering, presents the main data transfer control signals of the bus.
The STDINT mode, with default jumpering, presents primarily those signals related to interrupts.
In the STD24B mode, data lines 24...31 represent the upper 8 bits of a 24-bit address. These bits are clocked from the data bus into an octal register on the pod at the rising edge of the MCSYNC* bus signal; the outputs of this register drive data lines 24...31. None of the jumpering options affects the STD24B mode.
Early versions of the PM 3632 display these bits in two 4-bit binary fields.

5.3.3 JUMPERING OPTIONS

DATA LINES 24...31
In the STDBUS and STDINT modes, the signals presented on Data Lines 24...31 may be selected by the user. Any eight signals may be selected from the signals available at jumper posts to be displayed in either of these two modes. The table below shows the signals available, the mode/data-line destinations, and the default connections.

Source		Destination		
Signal -	Jumper pin	Jumper pin -	Mode -	Data Line
IOEXP/MEMEX	JP3- 1	JP3- 2	STDBUS	4
PCO	JP3- 3	JP3- 4	STDINT	4
BUSAK*	JP3- 5	JP3- 6	STDBUS	6
STATUS0*	JP3- 7	JP3- 8	STDINT	6
BUSRQ*	JP3- 9	JP3-10	STDBUS	5
REFRESH*	JP3-11	JP3-12	STDINT	5
WAITRQ*	JP3-13	JP3-14	STDBUS	7
STATUS1*	JP3-15	JP3-16	STDINT	7
MEMRQ*	JP4- 1	JP4- 2	STDBUS	3
PCI	JP4- 3	JP4- 4	STDINT	3
IORQ*	JP4- 5	JP4- 6	STDBUS	2
IORQ*	JP4- 7	JP4- 8	STDINT	2
RD*	JP4- 9	JP4-10	STDBUS	0
INTRQ*	JP4-11	JP4-12	STDINT	0
WR*	JP4-13	JP4-14	STDBUS	1
INTAK*	JP4-15	JP4-16	STDINT	1
SYSRESET*	JP5- 1			
PBRESET*	JP5- 2			
NMIRQ*	JP5- 3			
CLOCK*	JP6- 1			
CNTRL*	JP6- 2			

5.3.4 REFRESH CYCLES

During synchronous recording of bus cycles, the pod will record each Read cycle, each Write cycle, and each Interrupt Acknowledge cycle. Also, Refresh cycles may be recorded if a card on the bus supplies them. Either Z80 or NSC800 Refresh cycles may be captured, or Refresh cycles may be ignored according to the table below.

Refresh type	Jumpers Patch	
	-JP1-	-JP2-
Refresh ignored	2-3	2-3 (don't care)
Z80	1-2	2-3
NSC800	1-2	1-2

5.3.5 INTRQ AND BUSRQ*

When the Pod is used as an extender card, and the card plugged in is one which may issue INTRQ* and/or BUSRQ*, then the corresponding request signal available to the PM 3632 may be either the actual request signal on the STANDARD Bus, or the request signal emanating from the card. The table below shows the options available.

Request signal	Jumper patch -JP7-
BUSRQ* Source:	
Bus (default)	1-3
Card	3-5
INTRQ* Source:	
Bus (default)	2-4
Card	4-6

Note that, if the card must receive the request from the bus, then the request source must be the bus; the option of having the card as source is not available in that situation.

5.3.6 ASYNCHRONOUS OPERATION

When the Standard bus pod is used asynchronuously, the user should note that the signals travelling to the PM 3632 typically pass through two buffers (one high-speed CMOS buffer and one low speed buffer), plus a resistor network.

Since different signals pass through different buffers, the timing relationships between signals will be altered slightly, due to differences in path delays.
This timing skew should be less than 20 ns, with one exception: the address signals A0...15 are intentionally delayed approximately 20 nsec more than all other signals for proper synchronous operation with the Z80 STANDARD Bus.
The Z80 CPU, after an opcode fetch, very quickly outputs the refresh address, and without the delay, the address of the opcode fetch may not be captured properly at the clock edge occurring at the end of the fetch.
If this added delay in the address lines becomes annoying during asynchronous operation, change the resistor networks in Locations 5E and 6C to 270-ohm, individual-resistor networks (16 pins, 8 resistors). These locations are socketed. Save the original resistor networks for synchronous operation.

5.4 8-BIT MICROPROCESSOR PODS

5.4.1 GENERAL

These Pods are provided with a test clip, which directly connects to the microprocessor under test.
The brown wire of the colored ribbon cable must connect to pin 1 of the microprocessor.

A disassembly prom for the specific microprocessor is delivered with each Pod. For building-in refer to chapter 7.

Although all 8-bit micro-processor pods operate similarly, there are a few differences among them.

For all 8-bit micro-processors applies:
Data Inputs 0...7 are Data Bus Bits 0-7 (demultiplexed if required)
Data Inputs 8...23 are Address, although some bits (high-order) may not be used.
Data Inputs 24...27 are Status information
Data Inputs 28...31 are free input lines

Free data input lines:
On most micro-processor pods, some lines (generally four) are supplied as separate TTL inputs via a connector on the side of the pod. To use these TTL input lines, remove the 8-channel probe set from the 32-Channel Logic Pod (the 20-pin connector) and attach it to the connector on the side of the micro-processor pod.

Free data inputs color coding:

Input	Bit	Body(tip)	Plunger(cap)	Wire	Pinnr.
31	0	Black	Grey	Black	2
30	1	Black	Grey	Brown	3
29	2	Black	Grey	Red	5
28	3	Black	Grey	Orange	6
8031/32 only:					
27	4	Black	Grey	Yellow	8

Do not use the ground connections of this connector.

Clock signals are derived as required, from the signals on each micro-processor pod. Clock qualification is not used with micro-processor pods.

The PM 3632 will automatically configure itself at power-up for synchronous micro-processor cycle data collection, depending on the specific micro-processor. This configuration may however be changed, just as configurations may be changed with other pods.
The default trigger configuration has four fields : "BIN", a binary field for the extra data input lines : "STS" (Status) ; "ADR" (Address) ; and "DAT" (Data). These fields can be modified if desired. On the bottom of the screen are the status codes for easy reference.

Details of the data configuration for each particular micro-processor pod follow.

Connection check:

To detect a reversed pod connection error, the pod loads the target processor's V CC pin with 220 ohms.
If this 23 mA load is unacceptable, remove R7 from the pod's circuit board, or replace R7 with a resistor of a higher value.

5.4.2 PM 8865 MICROPROCESSOR POD

Supports Intel 8085, 8035/8039/8040, and 8031/8032.

Input channel numbering:

Line	Channel number	
Data bus 07--0	7--0	
Address bus A15--0	23--8	(19--8 for 8035/8039/8040)
Status lines	27--24	
Free inputs	31--28	(refer to 5.4.1)

Status lines:

	8085	8035/39/40	8031/32
#24=	S0	WR or PSEN	WR or PSEN
#25=	S1	RD or PSEN	RD or PSEN
#26=	IO/M	PROG	N.A.
#27=	HLDA	N.A.	N.A.

Microprocessor cycle types:

	Status lines: #27--24		
	8085	8035/39/40	8031/2
Fetch (or PSEN)	0011	X011	X011
Memory Read	0010	X010	X010
Memory Write	0001	X001	X001
I/O Read	0110	X1XX	N.A.
I/O Write	0101	X1XX	N.A.
Interrupt Acknowledgemen	0111	N.A.	N.A.
Hold Acknowledgment	1XXX	N.A.	N.A.

N.A.= Not Applicable

Switch setting (only for 8031/8032):

This switches are located at the same side as the auxiliary probe-connection.
Switches 1 and 2 select the 8031/8032 READ and WRITE signals as sample clocks.

Switch 1: Up READ signal not selected
Down READ signal selected

Switch 2: Up WRITE signal not selected
Down WRITE signal selected

Switches 3 and 4 are not used.

5.4.3 PM 8866 MICROPROCESSOR POD

Supports Motorola 6800, 6802, and 6808.

Input channel numbering:

Line	Channel number
Data bus D7--D0	7--0
Address bus A15--A0	23--8
Status lines	27--24
Free inputs	31--28 (refer to 5.4.1)

Status lines:

#24= R/W
#25= Halt
#26= VMA
#27= BA

Microprocessor cycle types:

	States lines: #27--24
Read	01X1
Write	01X0
Halt/Bus available	1X0X
Bus available	1XXX

SWITCH SETTINGS

For proper operation of the this micro-processor pod, follow the switch settings. The switches are located on the same side of the pod as the auxiliary probe connection, and are labelled 1, 2, 3 and 4. Up (toward the pod label) is open ; down is closed.

	6802, 6808	6800
Switch 1	Open	Write Clocking : Open--Fall of 02 Closed--Fall of DBE

Switches 2...4 are not used.

5.4.4 PM 8867 MICROPROCESSOR POD

Supports Motorola 6809 and 6809E.

Input channel numbering:

Line	6809 Channel number	6809E Channel number	
Data bus D7--0	7--0	7--0	
Address bus A15--0	23--8	23--8	
Status lines	27--24	29--24	
Free inputs	31--28	31--30	(refer to 5.4.1)

Status lines:

	6809	6809E
#24=	R/W	R/W
#25=	Halt	Halt
#26=	BS	BS
#27=	BA	BA
#28=	-	LIC
#29=	-	AVMA

Microprocessor cycle types:

	6809	6809E
Status lines:	#27--24	#29--24
Last instruction cycle	N.A.	X1XXXX
Read	00X1	XX00X1
Write	00X0	XX00X0
Interrupt acknowledg.	01XX	XX01XX
Sync. acknowledgment	10XX	XX110X
Bus grant due to halt	110X	XX110X
Bus grant	11XX	XX11XX

N.A.= Not Applicable

5.4.5 PM 8868 MICROPROCESSOR POD

Supports Rockwell 6502, 6512, 65C02, 65C102, and 65C112.

Input channel numbering:

Line	Channel number
Data bus D7--0	7--0
Address bus A15--0	23--8
Status lines	27--24
Free inputs	31--28 (refer to 5.4.1)

Status lines:

#24= R/W
#25= RDY
#26= SO
#27= SYNC

Microprocessor cycle types:

Status lines: #27--24		
Fetch	1X11	
Memory read	0X11	
Memory write	0XX0	(6502, 6512)
Memory write	0X10	(65C02, 65C102, 65C112)
Set overflow bit	X0XX	

SWITCH SETTINGS

For proper operation of this pod, follow the switch settings below.
The switches are located on the same side of the pod as is the auxiliary probe connector, and are labelled 1, 2, 3, and 4.
Up (towards the pod label) is open; down is closed.

	6502	65C02/102/112	6512
Switch 1	Open	Open	Write Clocking: Open : Use Switch 2 choice Closed: Fall of DBE
Switch 2	Open	Open	Read Clocking: Open : Fall of Ø2 Closed: Rise of Ø1
Switch 3	Closed	Open	Open
Switch 4	Open	Open	Closed

5.4.6 PM 8869 MICROPROCESSOR POD

Supports Zilog Z80/A/B/C.

Input channel numbering:

Line	Channel number
Data bus D7--0	7--0
Address bus A15--0	23--8
Status lines	27--24
Free inputs	31--28 (refer to 5.4.1)

Status lines:

#24= Write, or Fetch, or Interrupt Acknowledge
#25= Read, or Fetch, or Interrupt Acknowledge
#26= I/O, or Interrupt Acknowledge
#27= BUSAK

Microprocessor cycle types:

Status lines: #27--24	
Fetch	1011
Memory read	1010
Memory write	1001
I/O read	1110
I/O write	1101
Interrupt acknowledge	1111
Bus acknowledgment	0XXX
Refresh	1000

In the Z80 REF mode also the DRAM refresh-cycles activity is shown.

5.4.7 PM 8870 MICROPROCESSOR POD

Supports NSC800

Input channel numbering:

Line	Channel number
Data bus D7--0	7--0
Address bus A15--0	23--8
Status lines	27--24 (see below)
Reset	28
Free inputs	31--29 (refer to 5.4.1)

Status lines:

#24= S0
#25= S1
#26= IO/M*
#27= BACK*

Microprocessor cycle types:

Status lines: #27--24	
Halt	1000
Memory Write	1001
Memory Read	1010
Opcode Fetch	1011
Refresh	1100
I/O Write	1101

5.5 16-BIT MICROPROCESSOR PODS

5.5.1 GENERAL

Sample clocks:
Clock signals are derived as required, from the signals on each micro-processor pod. Clock qualification is not used with micro-processor pods.

Free input lines:
These Pods are provided with some free input lines, which can be used to sample data in addition to the microprocessor signals.
These signals are applied via the connector close to the ribbon cable pod-entry.
Do not use the ground connections of this connector.
Refer to the specific Pod description.

Logic Analyzer configuration:
The PM 3632 will automatically configure itself at power-up for synchronous micro-processor cycle data collection, depending on the specific micro-processor.
This configuration may however be changed, just as configurations may be changed with other pods.
The default trigger configuration has four fields :
-"BIN", a binary field for the extra data input lines
-"ST" (Status)
-"ADR" (Address) ; and
-"DAT" (Data).
These fields can be modified if desired. On the bottom of the screen are the status codes for easy reference.

Details of the data configuration for each particular micro-processor pod follow.

5.5.2 68000/68010 POD PM 8874

WARNING: THIS POD CONTAINS SEVERAL INTEGRATED CIRCUITS DISSIPATING A LARGE AMOUNT OF HEAT. DO NOT USE THE POD UNDER ANY CONDITION WHICH OBSTRUCTS THE NORMAL COOLING AIRFLOW AROUND IT.

1. GENERAL

A. SPECIAL REQUIREMENTS FOR THE PM 3632 TO ACCOMMODATE 16-BIT MICROPROCESSOR PODS

Revision L Base ROMs:
The PM 3632 base firmware must be Revision L or later.
(The top of the Status screen must be labeled "LB" or later.)

PM 8880/30 Disassembly ROM Board:
This board must be present in the PM 3632, and accommodates several 8- and 16-bit microprocessor disassemblers.

Two ROMs are supplied with the 68000/68010 pod:
-the Disa ROM, labelled "M6K00-*", specific for this pod
-the Trigger ROM, labelled "MT600-*", common for all 16-bit microprocessor pods.
Both ROMs must be installed on the PM 8880/30 Disassembly Rom Board inside the PM 3632 (* indicates the release number).

For installation instructions refer to chapter 7.2.

B. OPERATION

The Pod has been provided with a testclip, to connect directly to the microprocessor under test.
The brown wire of the colored ribbon cable must connect to pin 1 of the microprocessor.

The pod collects data (at up to 62 channels) at microprocessor clock speeds of up to 16 MHz, and formats it for logic analysis and full program disassembly (including all exceptions and bus cycles) by the PM 3632.

The Pod has three operating modes:
-Filtered,
-Transparent and
-Jump,
and produces disassembled code in each of them. Special hardware in the Pod tracks every bus cycle of the microprocessor and determines if the particular data will be recorded in the Pod's current operating mode.

In the Filtered mode, all unused prefetch cycles are removed in the pod hardware so they won't activate unwanted trigger events and won't be stored in the PM 3632 memory.

In the Transparent mode, all bus cycles are passed along to the PM 3632.

In the Jumpmode, all bus cycles are filtered out except for changes in program flow (branches, subroutine calls, exceptions, etc.), providing a disassembled "map" of how the code was actually executed.

The Disassembly display details all microprocessor data cycles ("unscrambled", and put back together with their corresponding instructions), provides labels for readability, and marks all instructions as either "u" for User or "s" for Supervisor, depending upon how they are fetched.
The State display shows data as it occurs on the address and data busses.
Data may also be viewed on the Timing display; however, there is no internal clocking capability, and only in the Transparent or Jump modes are samples stored in strictly increasing time order.
Filtered mode delays the storage of instruction cycles relative to that of data cycles.

If the microprocessor ceases operation (e.g., because of a HALT condition or a lack of DTACK, BERR, or VPA acknowledge during a bus cycle), several preceding bus cycles will remain stored in the pod. These cycles cannot be recorded or triggered upon until the microprocessor resumes operation.

2. HARDWARE

A. SWITCH SETTINGS

On one end of the PM 8874 Pod there is an access hole for a four-position DIP switch. This access hole is on the left end of the pod when viewed with the label lettering upright.

SWITCH 1 selects the processor type:

Down = 68000
Up = 68010 (To select the 68010, Switch 3 must also be Up.)

NOTE: PM 3632 power must be cycled (turned off, then on again) whenever the position of Switch 1 has been changed.

SWITCH 2 selects the data source for Probes 30, 29 & 28 (the leftmost three significant bits of the BIN field on the State display):

Down = the Interrupt Priority Level lines on the processor.
IPL2*, IPL1*, &IPL0*, active low, are Probes 30, 29 & 28, respectively)

Up = the external clip leads
Install the 20-pin lead set from the PM 8860 32-Channel Logic Pod in the 20-pin connector on the right end of the Pod.
Probes 30, 29 and 28 then correspond to leads 02, 01 and 00.

NOTE: The position of this switch may be changed during use; i.e., the power needn't be cycled (turned off, then on again).

SWITCH 3 selects the filtering type:

Down = 68000 systems without wait states or DMA cycles
Up = 68010 & 68000 systems with wait states or DMA cycles

Refer to Section 4, "Filtered Mode".

NOTE: The position of this switch may be changed during use.

SWITCH 4 is not used in this pod.

B. SIGNAL ASSIGNMENTS

Fifty-four signals are saved in each cycle of trace memory:

16 Data	lines	
24 Address	lines	The least significant address line is created by the hardware in the pod.
14 Discrete	lines	One of them is used for test and has no meaning to the user.

The data is saved in trace memory inverted, so the sense of the data displayed is automatically set to INV on the Format screen.
The probes are displayed in four groups (Address, Data, Status and other Binary).
The following tables relate probe numbers to signals and describe the signals.

Type	PM 3632 Probe Assign-ments	Default positions on Format Screen (See Fig. 5.1)	Significance
-	63	-	Not available for use
Status (STS)	62-56	5	Processor Status (Cycle ID)
Address (ADR)	55-32	6	Processor Address lines 0-23
	31	-	Not available for use
Binary (BIN)	30-24	1	See Binary Field, below
	23-16	-	Not available for use
Data (DAT)	15- 0	7	Processor Data lines 0-15

Signal assignments-overview table

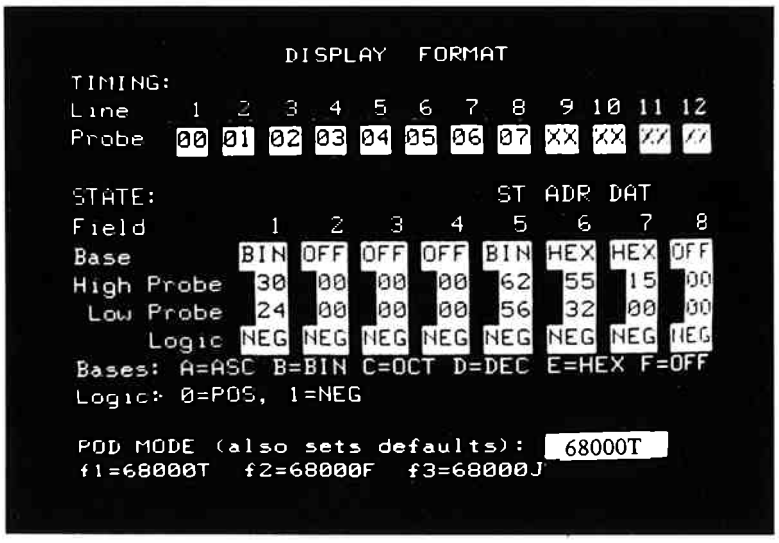


Fig. 5.1 *Display Format Screen*

Probe No.	Signal Description
Binary	(BIN) -- (field of 7 binary numbers)
30	IPL2*, or lead 02 if external signals are used
29	IPL1*, or lead 01 if external signals are used
28	IPL0*, or lead 00 if external signals are used
27	HALT*
26	(Used for test)
25	VMA*
24	BERR*
Status	(STS) -- (field of 7 binary numbers)
62	FETCH* or SOURCE, depending on Filtered or Jump mode (generated by the Pod)
61	BGACK*
60	BYTE
59	R/W*
58	FC2
57	FC1
56	FC0
Address	(ADR) -- (field of 6 hexadecimal numbers)
55-52	A23-A20
51-48	A19-A16
47-44	A15-A12
43-40	A11-A08
39-36	A07-A04
35-32	A03-A00
Data	(DAT) -- (field of 4 hexadecimal numbers)
15-12	D15-D12
11-8	D11-D08
7-4	D07-D04
3-0	D03-D00

Detailed signal assignments table

---

* denotes an activ low signal

To change the format of the State display (including number base), refer to chapter 3.8, "Format Setup Screen".

Default number bases for the State display are:

Field	Base
Binary (BIN)	Binary
Status (STS)	Binary
Address (ADR)	Hexadecimal
Data (DAT)	Hexadecimal

Default number bases for displays

Signal	Logic	Function
BGACK*	'0'	Non-processor cycles, such as DMA
BYTE	'1'	8-bit transfers
R/W*	'0'	Write
	'1'	Read
VMA*	'0'	Autovectored interrupts or special hardware interface, e.g., 68000-type peripherals
BERR*	'0'	Bus error
HALT*	'0'	and BERR* also '0', indicates cycle is to be retried
FETCH*	'0'	First word of an instruction (Filtered mode only)
SOURCE	'1'	Source-address of a program discontinuity (Jump mode only)

Quick reference list for some status and binary signals

Probe 62: FETCH* is created by the pod in the Filtered mode, it is asserted during the first cycle of an instruction.
SOURCE is created by the pod in the Jump mode.
It is high if the cycle is a Source, and low if it is a Destination. If the cycle is both a Destination and a Source, the bit will be low. In the Filtered mode, this bit indicates the first word of an instruction fetch.

Probe 61: BGACK* is the Bus Grant Acknowledge input to the processor. When low, cycles are performed by a device other than the processor. In the Filtered mode, such cycles are removed from the data stream. In the Transparent mode, any BGACK* cycles in the memory are ignored by the disassembler.

Probe 60: BYTE is created by pod hardware; it is high when only one data strobe is asserted.

Probe 59: R/W* is the READ/WRITE* signal from the processor; it is high during Read cycles and low during Write cycles.

Probes 58-56: FC2, FC1 and FC0 are the processor function codes which indicate which of several address spaces is accessed by a given cycle. Refer to 'Function Codes', below.

Probe 32: A0 is created by the Pod hardware.
It is high when the lower datastrobe (LDS) is asserted and the upper data strobe (UDS) is negated.

Probes 30-28: Lead 02, Lead 01 & Lead 00 or IPL2*, IPL1* & IPL0 (Interrupt Priority Level lines), depending upon whether the position of Switch 2 on the Pod is Up or Down, respectively. Refer to "Switch Settings", above.

Probe 27: HALT* -- See Probe 24, BERR*.

Probe 26: Used for test, and underfined for normal operation.

Probe 25: VMA* is the Valid Memory Address output from the processor, asserted in response to the VPA* (Valid Peripheral Address) signal. These signals are used primarily when interfacing to 6800-type peripherals.
If VPA* is asserted by external hardware during an Interrupt Acknowledge cycle, the processor performs an autovector operation.
Note that data sampling is different during VMA* cycles, using the falling edge of E rather than the rising edge of the data strobes. Refer to the microprocessor handbooks for details.

Probes 24-27: BERR* and HALT* signals are taken directly off the processor. When the BERR* signal is asserted without HALT*, the processor takes a bus error exception; when BERR* and HALT* are both asserted, the processor will retry the cycle. In the Filtered mode, cycles with both BERR* and HALT* asserted (cycles to be retried) are removed, as the cycle will recur.

Detailed list of binary and status signals

C. FUNCTION CODES

The BIN (Binary) and STS (Status) fields (on the default Trigger screen and State display screen) contain status information about the bus cycle. The three least significant bits of the STS fields are the function codes FC2, FC1 and FC0 of the processor, which define the "space" of the cycle as shown:

FC2	FC1	FC0	Cycle Space
0	0	1	User Data
0	1	0	User Program
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	CPU; used for Interrupt Acknowledge and Breakpoint cycles

Other combinations are unassigned and cannot be accessed in the 68000, the 68010 can access them via the MOVES instruction.

An abbreviated list of the BIN and STS signals is available on the TRIGGER Setup Screen, shown below.

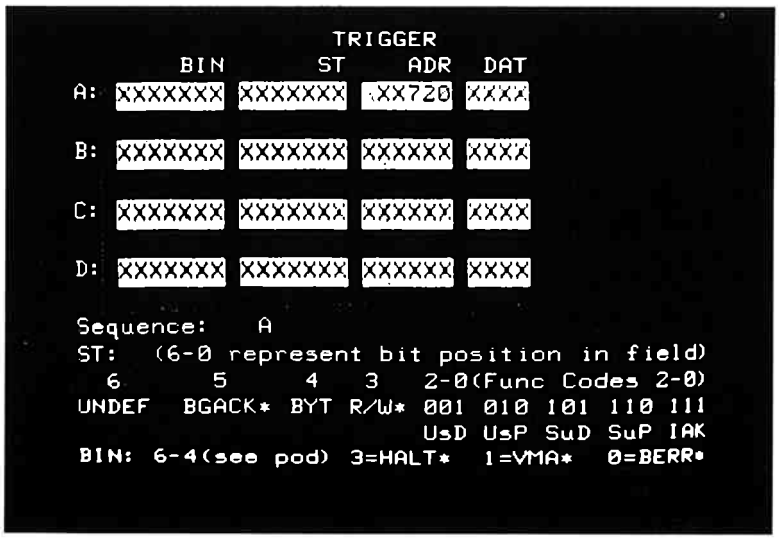


Fig. 5.2 *Trigger Screen with PM 8874 Pod*

Acces type	STS
READ User Data Space Word	X101001
WRITE User Data Space Word	X100001
READ User Data Space Byte	X111001
READ User Program Space Word	X101010
READ User Program Space First Instruction Word (Filtered mode only)	0101010
READ Supervisor Program Space First Instruction Word	0101110
WRITE Supervisor Data Space Byte	X110101
Interrupt Acknowledge (The level of the interrupt being acknowledged is available on Address Lines A3, A2 and A1. Also, in the 68010, Interrupt Acknowledges must be distinguished from breakpoints by using upper address lines).	X101111

Special Cycles	BIN	STS
Autovectored Interrupt Acknowledge (VMA* asserted in response to VPA*)	XXXXX0X	X101111
Bus Error Cycle	XXX1XX0	X1XXXXX
Retry Cycle (Transparent mode only)	XXX0XX0	X1XXXXX
VMA* Cycle (special hardware)	XXXXX0X	-
Non-processor Cycle (DMA)	XXXXXXX	X0XXXXX

Status code examples

3. TRANSPARENT MODE

In the Transparent mode, all bus cycles (including unused pre-fetches) are sent to the PM 3632 logic analyzer in the order in which they occur. Data captured in the Transparent mode can be viewed in all three display formats: State, Timing and Disassembly.
The disassembler discards unused pre-fetches, so that disassembled data is the same, as it is in the Filtered mode.

See also Sections 6.C, "Undesired Triggering on Pre-fetches in Transparent Mode", and 4.B.b, "FIFO Memory".

4. FILTERED MODE

A. GENERAL

As with most 16-bit microprocessors, the 68000 uses an instruction pre-fetch mechanism to enhance performance. While one instruction is being executed, the two words following it have already been fetched from program memory. If an instruction or exception causes a branch, one or both of the pre-fetched words will be discarded.
With logic analyzers that fail to filter pre-fetched words, triggering on a location in program memory guarantees only that the instruction has been fetched, not executed.

To eliminate undesired triggering, the PM 8874 Microprocessor Pod tracks every bus cycle and filters out unused prefetches from the instruction stream sent to the PM 3632 Logic Analyzer.
Increased data storage is an added benefit of filtering, because unused pre-fetches do not take up any space in the 500-cycle trace memory of the PM 3632.

Data captured in the Filtered mode may be displayed in State, Timing and Disassembly formats.

B. HARDWARE CONSIDERATIONS

a. General

When in Filtered mode, special hardware in the PM 8874 Microprocessor Pod monitors the processor's bus cycles to determine when prefetched cyles have not been executed.
Because as many as thirty bus cycles may occur between the read of an instruction and its execution (or its being discarded), the Pod must temporarily hold the instruction off to one side of the data stream until it has enough information to determine whether the cycle has actually been executed.

The result is that (in Filtered mode) all instruction words appear in the PM 3632 memory and in the State display where the next instruction word would have appeared if in Transparent mode, except for instruction words which are found to be unused prefetches, which are removed completely.

Note that, due to the delay of Filtered mode, the cycles appear in the PM 3632 memory in the same order in which the processor actually performed them, not in the order in which they were fetched off of the bus by the pre-fetch mechanism. This may be important to the user when viewing external signals or interrupt levels on the State display.

b. FIFO Memory

In Filtered mode, a small (4-cycle), first-in-first-out memory in the Pod removes cycles in the event of an interrupt, when two pre-fetched cycles are discarded.
If the processor stops execution, this FIFO memory will contain the last four cycles and they will not have been captured in the PM 3632 trace memory.
In Transparent mode, the length of this FIFO memory is reduced to one cycle.

c. Unremoved Pre-fetches

Three instructions (CHK, DIV and TRAPV) and the TRACE exception generate exceptions in a way that makes it difficult to remove all pre-fetches; in fact, it is sometimes impossible to know whether one or two pre-fetches need to be removed.
In these cases only one pre-fetched word (the last) is removed.

Address and Bus Error exceptions do not have unused pre-fetches, but a cycle may be deleted anyway. The address of this cycle is pushed on the stack and labeled "AA" (see Section 7.C.c, "Exceptions"), so the loss of this cycle should not pose a problem.

Another ambiguous circumstance occurs when the processor executes a single-word conditional branch around a one-word instruction that makes no data accesses.
The difficulty arises because the data stream is identical, regardless of whether or not the branch is taken.
In the 68010, the execution speed is also identical, regardless of path, and so it is not possible to know whether the one-word instruction has been executed.
The 68000 takes two clock cycles longer when the instruction has been executed than when it has not been executed, and the Pod monitors this in order to decide whether or not the instruction has been skipped and is to be discarded.
The clock cycle counting information may not be valid in systems with wait states or in which DMA cycles can occur. In either case, the one-word instruction following the branch is marked with a "?" in the disassembly display to indicate the uncertainty about its actual execution.

The usage of the cycle counting information is controlled by the user, via Switch 3 on the Pod.
For 68010 systems, this switch must be Up, or all such instructions will be removed.
For most 68000 systems, this switch should be Down.
For 68000 systems with DMA or wait states, the switch should usually be Up.
The switch may be Down, but the user must be aware of the possibility of cycles being filtered out which have actually been executed.

d. Self-Synchronization

In order to make intelligent decisions about unused prefetches, the Pod must synchronize itself with the processor.
Under ordinary circumstances,only a few cycles are required for synchronization, and it will actually self-synchronize before the PM 3632 begins recording data.

There are certain patterns of instructions for which the pod is not guaranteed to synchronize itself, but such patterns are virtually always tight loops of fewer than ten unusual instructions with no writes.
If such a pattern occurs,the pod may incorrectly remove cycles from the data stream, and the user must either use the Transparent mode, or restart data acquisition in the Filtered mode in hopes that the pod will synchronize itself. Such self-synchronization may indeed occur, because synchronization may depend upon the exact point in the pattern at which acquisition begins.
A processor RESET will cause the pod to lose sync.
It should resynchronize within a few cycles, but for analyzing the processor's behavior at RESET, the Transparent mode is recommended.

5. JUMP MODE

The Jump mode filters out all bus cycles, except those preceding and following events that cause changes in program flow (such as branches, subroutine calls and exceptions). This feature is very usefull for checking program flow and determining which sections of code are being executed. Data captured in the Jump mode can be viewed in all three display formats: State, Timing and Disassembly.

The Disassembly display screen describes each entry as a Source ("was branched from-") or Destination ("was branched to-").
Since only the first word of each instruction is stored in the analyzer, only the mnemonic of each instruction is displayed.
If an instruction is both a Destination and a Source (e.g., when a jump lands at another jump), the instruction appears only as a Destination in the state buffer (i.e., no source entry is recorded, and there will be two Destination entries in a row). Thus, it is always posssible to set a trigger on a Destination, but those Source instructions which are also Destinations will never be recorded with the "SOURCE" bit set in the STS field.

6. TRIGGERING

A. TRIGGERING SEQUENCE LIMITATIONS IN 62-BIT OPERATION

The basic width of the PM 3632 data path is 32 bits.
In order to accommodate 16-bit processors, the PM 3632 divides a processor-cycle into halves, and these halves are stored sequentially.
One bit of each set of 32 bits marks which, leaving 31 bits per half and a total of 62 bits.

The basic triggering mechanism in the PM 3632 is also 32 bits wide and has up to 13 states. When only the upper 31 bits of information (Status and Address fields) are used, all triggering capabilities are available (as described in chapter 3.5, 3.6 and 3.7).
However, it is often necessary to use the Binary and Data fields to trigger. Special software allows the user to specify a single 62-bit trigger word.

In general, the software allows the user to be unconcerned with the triggering width of the machine; there are, however, some limitations. Some complex sequences required too many states to be implemented in the 13-state sequence machine.
For example, the Trigger Sequence "A+B+C+D" requires 16 states to represent the condition past the first half of the trigger word, so this sequence is unavailable when Binary and Data fields (other than "Don't Cares") are specified. "Without" conditions also add complexity.

All of the PM 3632's predefined sequences except "A+B+C+D" are available. For that sequence and for a User-Defined Sequence, the number of states needed for a given condition level can be calculated using these rules:

A single word requires two states.
If further words are "ORED" in, double the number of states for each additional "true" word (e.g., A as opposed to A*).
If words are "ANDed" in, double for each additional "not" word (e.g.,A*).
Examples of number of states required for a given condition level are:

Condition	No. of States
A	2
A + B	4
A + B + C*	4
A & B	2
A* & B*	4
A + B + C	8
A* & B* & C*	8

Number of states per trigger condition

Each level consists of two conditions; (refer also to Fig. 3.6).
-add the number of states required for each set of two conditions
-multiply the resultant sum by the count for that level.
-sum at each level to obtain the total number of states.

However, it is usually not worth the effort to determine the number of states required by a particular sequence, because the 62-bit trigger and sequence software determines whether the specified sequence is too complex. Simply enter the sequence via the TRIGGER SEQUENCE screen, and the PM 3632 software will decide whether the sequence is too complex.
If it is, the PM 3632 will display an error message ("TRIGGER TOO COMPLEX") on the STATUS screen; just remove a word from a condition or reduce the count at a level, and try it again.

B. DATA QUALIFICATION

Due to the 32-bit nature of the PM 3632 capture and trigger circuitry, only the first 31 bits (the default Status and Address fields) of a processor cycle may be used to qualify data storage. Thus cycles may be qualified based on Address and access type, but not on the Data field.
Although the qualification decision is based on the first (upper) half of the cycle, the same decision holds for the second (lower) half of the cycle; i.e., whole 62-bit frames are either qualified or not qualified.

C. UNDESIRED TRIGGERING ON PREFETCHES IN TRANSPARENT MODE

In the Transparent mode, prefetched instructions which are not executed, may cause undesired triggering, i.e., triggering of the logic analyzer without the occurence of the event of interest.
Such unused pre-fetches are found before interrupts, after branches and returns, and sometimes after jumps and calls.
Because these instructions have not been executed, they will not appear on the Disassembly screen.

To avoid undesired triggering, use the Filtered mode, which strips unused pre-fetches from the data stream (described in Section D, "Filtered Mode").

Also the following methods may be used to simplify the trigger behaviour.

Method 1:
-If possible, set the trigger word to an instruction downstream from the over-fetched instruction, but in the same execution path.
To avoid false triggering, this downstream instruction must be far enough away from the cause of the over-fetching (a jump, call, return, software interrupt, or other interrupting instruction) that the over-fetching does not reach the downstream instruction.

Method 2:
-Trigger on a non-instruction data access unique to the instruction desired, or another instruction in the same code path.
Unexecuted instructions do not perform any non-instruction data accesses.

Method 3:
-Trigger on a sequence of instruction fetches and/or data accesses unique to the code path desired.

7. DISPLAY

A. GENERAL

With the PM 8874 Pod in Transparent mode, the State display shows all instruction fetches and data cycles in the same order in which they occured on the bus.
In the Filtered mode, the order of cycles in the trace memory will not match the actual order of cycles on the processor bus (see Section D, "Filtered Mode"), and any unused fetches (fetches following an instruction causing a program discontinuity) are disqualified by the Pod and not stored in the trace memory.

The Disassembly display groups these program fetches and data cycles into 68000 assembly language instructions.
Regardless of whether or not the Pod is filtering unused fetches, these unused fetches are not displayed on the Disassembly screen.
The current Pod mode is shown in a reversed-video field at the top of the Disassembly screen.

The formatting and display of data is described generally for the PM 3632 in chapters 3 (SET UP SCREENS) and 4 (DATA DISPLAYS).

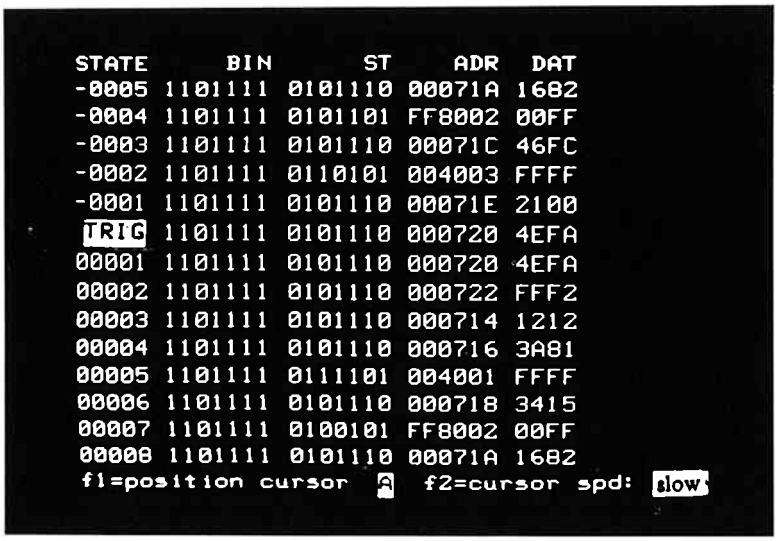


Fig. 5.3 *Date Display (all modes)*

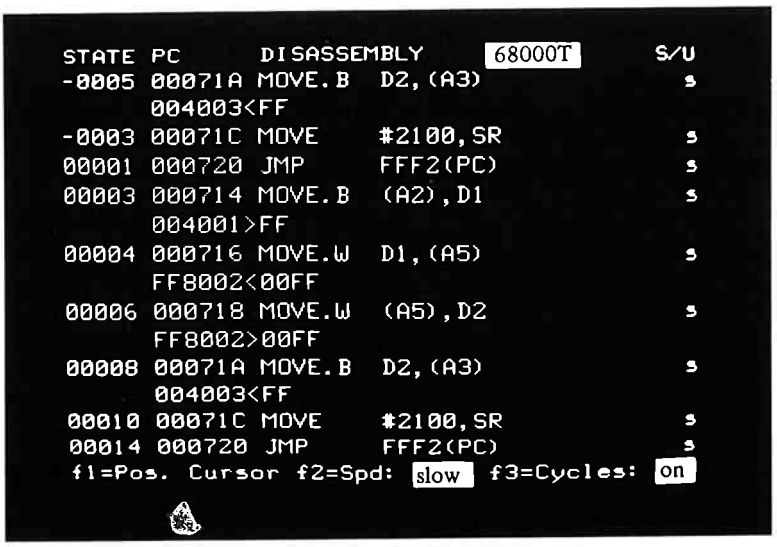


Fig. 5.4 *Disassembly Display (Transparent and Filtered Modes)*

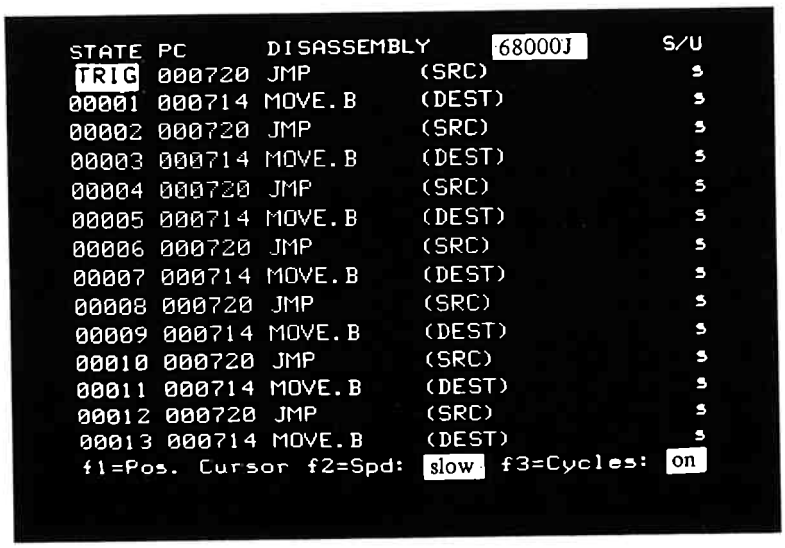


Fig. 5.5 *Disassembly Display (Jump Mode)*

B. KEY FUNCTIONS ON THE DISASSEMBLY SCREEN

f1 Key (Position Cursor):
To move directly to any location in the memory:
-depress the f1 key,
-enter the state number you wish to display,
-depress f1 again.
Negative state numbers correspond to cycles before the trigger event, positive state numbers correspond to cycles after the trigger.
If f1 is inadvertently depressed, depress it again to leave the cursor at its current location.

Up/Down Arrow Keys (Scroll through the memory):
To move through the memory forward or backward, use the Up and Down Arrow keys.

f2 Key (Scroll Speed):
To scroll slowly through the memory (one instruction at a time), use the f2 key to set the scroll speed to Slow.
To scroll faster, toggle the f2 key to set the scroll speed to Fast.

f3 Key (Data Cycles On/Off):
To view the disassembled instructions without their associated data cycles, depress the f3 key. This gives a display very similar to an actual code listing and makes it easier to locate a particular section of code.
To turn the data cycles back on, toggle the f3 key.

f4 Key (Print Screen):
To print a hardcopy report of the Disassembly screen, depress the f4 key. There is no on-screen prompt for this function.
Note that the RS-232C option must be installed; this is included in the ROM Emulator Module, PM 8880/00.

DISAM Key (Display Trigger Condition):
To display the trigger event, depress the DISAM key once to enter the Disassembly screen and again to display the trigger event.

C. DISASSEMBLY DISPLAY FORMATS

a. Instruction Display

As with 8-bit microprocessor pod disassembly, each instruction displayed contains a state number corresponding to the instruction position relative to the trigger event, the value of the Program Counter when the instruction was fetched (PC), and the mnemonic and operands for the instruction itself. Also with the 68000/68010 pod, an "s" or "u" at the far right of the screen indicates whether the instruction was fetched from Supervisor space or from from User space.

b. Data Cycles Display

Data cycles are displayed on lines following the instruction that caused. them. Display of these cycles may be turned on or off by toggling the f3 key.

Each data cycle contains an address, an indication of whether data was read from (>) or written to (<) the address, and the data itself.
Each address consists of six hexadecimal characters (24 bits), while data may be a byte (2 characters), a word (4 characters), or a long word (8 characters).

Even though the 68000 performs a long word access by doing two word accesses, the PM 3632 concatenates the data and shows it as as one data cycle on the Disassembly screen.

c. Specific Instruction Display Techniques

MOVEM

The register list coded with the MOVEM instruction is reconstructed, and shown as the second line of the instruction.
This line is part of the instruction and stays displayed even with data cycles off.
The data cycles associated with the MOVEM instruction are in the same order (reading left to right) as they are on the register list. (See Figure 5.4, "Disassembly Display, Transparent and Filtered Modes".)

BSR, JSR

The data cycle showing the value of the Program Counter pushed onto the stack is labelled "PC:".

RTD, RTS, RTR

The data cycle showing the value of the Program Counter popped from the stack is labelled "PC:".

EXCEPTIONS

a) PC, SR, VO, IR, AA Labels

The data cycles showing the values of the Program Counter and Status Register pushed onto the stack are labelled "PC:" and "SR:", respectively.
If the processor is a 68010, the data cycle showing the Vector Offset is labelled "VO:".
On a 68000 bus error or address error exception, the data cycle showing the Instruction Register push is labelled "IR:" and the cycle showing the Access Address push is labelled "AA:".

b) 68010 Bus or Address Error Exception

On a 68010 bus error or address error exception, the following data cycles are labelled:

FA:	Fault Address
DO:	Data Output Buffer
DI:	Data Input Buffer
II:	Instruction Input Buffer

c) Unlabelled Cycles

Unlabelled cycles correspond to Motorola internal information.
See Motorola M68000 Programmer's Reference Manual, M68000UM(A)D4, for additional information.

d) Interrupts

If the exception is an interrupt, then the type of interrupt (externally vectored, autovector, spurious or uninitialized), interrupt priority level and interrupt vector number are displayed and labelled as such.

e) Exception Vector

All exceptions label the exception vector which is read as "VECTOR:".

8. DISASSEMBLY MESSAGES

The Disassembly software displays only executed (as opposed to pre-fetched) instructions, regardless of whether the pod is in the Filtered mode (sending up only executed cycles) or Transparent mode (sending up all cycles).

To do this, the disassembly software must "sync up" to the cycles in the trace memory, in much the same way as the pod hardware syncs up to the processor in the Filtered mode.
The disassembly software finds the first program space read, assumes it is an opcode fetch and checks the following cycles to see if it made a correct assumption. If the following cycles don't match the expected pattern of instruction fetches, data cycles and prefetches for that particular opcode value, then the software assumes it found a subsequent byte of an instruction or a program space operand read. It ignores this cycle, finds the next program space read and repeats the process.

This software process of syncing up to the trace cycles is performed in both the Transparent and the Filtered modes.
This seems unnecessary in Filtered mode, because the pod sends up information identifying the first word of an instruction.
Data qualification, however, may filter out subsequent cycles of an instruction, so that relying upon the fetch bit may be insufficient.

If the software cannot make sense of the cycles in the memory, it will display the message "CAN'T DISASSEMBLE--PS READS USED AS OPCODES".
It then shows disassembly of the memory, assuming that every PS (= Program Space)-read was the first word of an instruction.
Each line of display is marked with a "?" to indicate the software's uncertainty with the disassembled code.

If the software cannot make sense out of some of the cycles in the memory, but then can resync to the trace cycles, it displays the message "UNABLE TO DISASSEMBLE XXX CYCLES", where "XXX" is the number of processor cycles that did not fit the expected pattern.

In addition, a special case exists when a one-word instruction with no data cycles follows a conditional branch instruction. The processor cycle pattern appears identical, whether or not the branch has actually been taken.
The software cannot determine whether or not the instruction has been executed, so it marks it with a "?".

5.5.3 8086/8088 POD PM 8876

WARNING: THIS POD CONTAINS SEVERAL INTEGRATED CIRCUITS DISSIPATING A LARGE AMOUNT OF HEAT.
DO NOT USE THE POD UNDER ANY CONDITION WHICH OBSTRUCTS THE NORMAL COOLING AIRFLOW AROUND IT.

This Pod fully supports Intel 8086 and 8088 microprocessors, and the Intel 8087 co-processor, including disassembly.
It partially supports the Intel 8089 co-processor by collecting data, but without disassembly.

If the Pod is to be clipped onto an 8087 or 8089 directly, a hardware jumper inside the Pod must be moved; see Section 2.0, ("Pod Connection Error Warning").

1. GENERAL

A. SPECIAL REQUIREMENTS FOR THE PM 3632 TO ACCOMMODATE 16-BIT MICROPROCESSOR PODS

Revision "L" Base ROMs:
The PM 3632 base firmware must be Revision "L" or later.
(The top of the Status screen must be labeled "LB" or later.)

PM 8880/30 Disassembly ROM Board:
This board must be present in the PM 3632, it accommodates several 8- and 16-bit microprocessor disassembler ROMs.

Two ROMs are supplied with the 8086/8088 Pod:
-the Oisa ROM, labelled "M8600-*", specific for this pod.
-the Trigger ROM, labelled "MT600-*", common for all 16-bit micro-processor pods.
Both ROMs must be installed on the PM 8880/30 Disassembly Rom Board inside the PM 3632 (* indicates the release number).

For installation instructions refer to chapter 7.2

B. OPERATION

The Pod has been provided with a testclip, to connect directly to the 8086 or 8088 under test.
The brown wire of the colored ribbon cable must connect to pin 1 of the microprocessor.

The pod collects data (at up to 62 channels) at microprocessor clock speeds of up to 10 MHz, and formats it for logic analysis and full program disassembly (including all exceptions and bus cycles) by the PM 3632.

The 8086 and 8088 have two operating modes: Minimum and Maximum.

Minimum mode:
The processors provide few indications of their internal operation; in particular, no indication of instruction queue activity is available outside the processor.
For Minimum mode processors, the PM 8876 Pod works only in the Transparent mode.

Maximum mode:
The processors provide queue status information for use by co-processors.
In the Maximium mode three Pod operation modes are possible:
-Transparent
-Filtered
-Jump
The filtered and jump modes use the queue status information to record only specific processor cycles.

There are a total of eight combinations of processor modes and Pod modes, and the disassembler Prom produces disassembled code in each of them.

In the Transparent mode, all bus cycles are passed along to the PM 3632.

In the Filtered and Jump modes, special hardware in the Pod tracks every bus cycle of the microprocessor, and determines if the particular data will be recorded in the Pod's current operating mode.

In the Filtered mode, all unused pre-fetch cycles are removed in the Pod hardware, so they won't activate unwanted trigger events and won't be recorded in the PM 3632 memory.

In the Jump mode all bus cycles are filtered out except for changes in program flow (jumps, subroutine calls, interrupts, etc.), resulting in a disassembled "map" of where code was actually executed.

The Disassembly display screen details all microprocessor data cycles "unscrambled" and put back together with their corresponding instructions.
The State display screen shows data in the order in which it was transmitted by the Pod.
Data may also be viewed on the Timing display; however, there is no internal clocking capability, and only in the Transparent or Jump modes are samples stored in increasing time order.
Filtered mode delays storage of instruction cycles relative to that of data cycles.

2. HARDWARE

A. SWITCH SETTINGS

On one end of the PM 8876 Pod there is an access hole for a four-position DIP switch. This access hole is on the left end of the pod when viewed with the label lettering upright.

SWITCH 1 selects the processor mode:

Down = MAX (Maximum mode)
Up = MIN (Minimum mode)

NOTE: PM 3632 power must be cycled (turned off, then on again) whenever the position of Switch 1 has been changed.

SWITCH 2 selects the data bus width (processor type):

Down = 8 bits (8088 processor)
Up = 16 bits (8086 processor)

NOTE: PM 3632 power must be cycled (turned off, then on again) whenever the position of Switch 2 has been changed.

SWITCH 3 controls instruction byte repacking, and applies to the use of the Filtered Pod mode on 16-bit processors (8086F) only:

Down = Repack instruction bytes into words before recording.
Unless a data cycle occurs on the processor bus after the low-instruction-byte is used and before the high-instruction-byte is used.
Up = Send instruction bytes to the PM 3632 as soon as they are used.
Make no specific attempt to repack the bytes. Repacking may occur occasionally.

NOTE: This switch must be normally Down, or the disassembler may be unable to disassemble portions of the recorded data.
The switch-setting may be changed during use. Refer to chapters 5.B and 7.C.

SWITCH 4 controls the Jump mode operation for max-mode processors only.

Down = Jump mode records only program flow discontinuities due to INTR interrupt.
Up = Jump mode records program flow discontinuities due to all causes (jumps, calls, returns, software- and hardware interrupts, and instruction traps).

NOTE: The switch-setting may be changed during use.
The setting of this switch should be examined (and changed if necessary) whenever the user chooses to operate the Pod in the Jump-mode. Refer to section 6.

B. SIGNAL ASSIGNMENTS

The signal assignments vary with the Pod mode, which is dependent upon the processor type (8086 and 8088) and processor mode (Minimum or Maximum). The following table lists the 8 combinations of processor modes and Pod modes, and show how they ared designated on the PM 3632 display screen.

Modes Design.	Processor Mode	Data Bus Width (bits)	Pod Recording Mode
8086mn	Minimum	16	Transparent
8086T	Maximum	16	Transparent
8086F	Maximum	16	Filtered
8086J	Maximum	16	Jump
8088mn	Minimum	8	Transparent
8088T	Maximum	8	Transparent
8088F	Maximum	8	Filter
8088J	Maximum	8	Jump

Designations of the PM 8876 pod modes

Signals class assignments for the 62 available probe lines (62--32, 30--0) are:

BINARY		ALL MODES: Probe 18 = Side Probe 1 Probe 17 = Side Probe 0 Probe 16 = Reset Flag
STATUS	BOTH MINIMUM MODES: (8086mn & 8088mn) Probes 60--52	ALL MAXIMUM MODES: (8086T, 8086F, 8086J, 8088T, 8088F, 8088J) Probes 62--52
ADDRESS		ALL MODES: Probes 51--32 (32= LSB)
DATA	ALL 8086 MODES: (8086mn, 8086T, 8086F, 8086J) Probes 15--0 (0= LSB)	ALL 8088 MODES: (8088mn, 8088T, 8088F, 8088J) Probes 7--0 (0= LSB)

Signal class assignments-overview

Probe No.	Label on Trigg screen	8086mn	8086T	8086F	8086J
52	B0	BHE*	BHE*	BHE*	BHE*
53	B1	PHLD	LOCK*	LOCK*	LOCK*
54	B2	IAK*	S0*	S0*	S0*
55	B3	DT/R*	S1*	S1*	S1*
56	B4	M/IO*	S2*	S2*	S2*
57	B5	S3	S3	S3	S3
58	B6	S4	S4	S4	S4
59	B7	S5	S5	S5	S5
60	B8	S6(=0)	S6	S6	S6
61	B9	--	(1)	FL*	ID*
62	B10	--	(1)	FH*	SRC

Probe No.	Label on Trigg screen	8088mn	8088T	8088F	8088J
52	B0	BHE*	BHE*	BHE*(=1)	BHE*(=1)
53	B1	PHLD	LOCK*	LOCK*	LOCK*
54	B2	SS0*	S0*	S0*	S0*
55	B3	DT/R*	S1*	S1*	S1*
56	B4	IO/M*	S2*	S2*	S2*
57	B5	S3	S3	S3	S3
58	B6	S4	S4	S4	S4
59	B7	S5	S5	S5	S5
60	B8	S6(=0)	S6	S6	S6
61	B9	--	(1)	FL*	ID*
62	B10	--	(1)	(1)	SRC

Status signal assignments

(1) is always '1'

Most status signals are sampled directly at the microprocessor, and their names correspond directly to 8086 or 8088 signals.

---

* denotes an active low signal.

Those status signals whose names do not correspond to 8086 or 8088 signals are below:

PHLD	is high (1) for the first recorded microprocessor-caused bus cycle following an occurrence of HLDA. This signal is present in minimum mode only, and indicates that a DMA cycle (or cycles) probably occurred just prior to this microprocessor cycle. DMA cycles are not recorded in trace memory for minimum-mode processors.
IAL*	is low (0) for INTA* cycles, and is an approximate substitute for S0*, which is not available on the minimum mode 8086.
FL*	is low (0) if the lower data byte is the first byte of an instruction.
FH*	is low (0) if the upper data byte is the first byte of an instruction.
SRC	is high (1), for 8086J and 8088J modes, if the indicated byte on the data bus is the Source of a discontinuity, and low (0) if the byte is the Destination of a discontinuity.
ID*	is low (0), for 8086J and 8088J modes, if this Destination entry in trace memory is due to a discontinuity caused by an INTR hardware interrupt.

Status signals whose names do not correspond to 8086/8088 signals

Probe No.	Signal	Function
18	Side Probe 1	Sampled about 12 ns after the processor data bus is sampled (at the end of each bus cycle)
17	Side Probe 0	
16	RESET	A latched signal set on the first bus cycle following reset (fetch at 0FFFF0H)

Binary field signal assignments

C. STATUS CODES

The STS field (on the Trigger setup- and the State display screens) specifies status information about processor bus cycles.
The signals on Probes 56--54 (usually processor signals S2*, S1* and S0*) specify the purpose of the cycle (I/O read, I/O write, memory read, memory write, fetch, or interrupt acknowledge).
The following table shows status codes for the various types of cycles.

STATUS	ALL MAX. MODE PROCESSORS	8088mn	8086mn
Interrupt Acknowledge	XXXXXX 000XX	XXXX 000XX	XXXX 000XX
I/O Read	XXXXXX 001XX	XXXX 001XX	XXXX 001XX
I/O Write	XXXXXX 010XX	XXXX 010XX	XXXX 011XX
Fetch (except 8086mn)	XXXXXX 100XX	XXXX 100XX	-
Fetch (8086mn)	-	-	XXXX 101XX
Memory Read (Fetch in 8086mn)	XXXXXX 101XX	XXXX 101XX	-
Memory Write	XXXXXX 110XX	XXXX 110XX	XXXX 111XX

Typical status codes for triggering on specific cycle types

The signals on Probes 58 and 57 (S4 and S3) indicate which segment of memory was accessed by the bus cycle. The following examples specify memory segments in addition to cycle type.

ACTION	ALL MAX. MODE PROCESSORS	8088mn	8086mn
Read from ES	XXXX00 101XX	XX00 101XX	XX00 101XX
Read from SS	XXXX01 101XX	XX01 101XX	XX01 101XX
Read from CS	XXXX10 101XX	XX10 101XX	XX10 101XX
Read from DS	XXXX11 101XX	XX11 101XX	XX11 101XX
Write to ES	XXXX00 110XX	XX00 110XX	XX00 111XX
Write to SS	XXXX01 110XX	XX01 110XX	XX01 111XX
Write to CS	XXXX10 110XX	XX10 110XX	XX10 111XX
Write to DS	XXXX11 110XX	XX11 110XX	XX11 111XX

Typical status codes for triggering on specific memory segment accesses

By Intel convention, the signals on Probes 60 and 59 (S6 and S5) indicate the following:

If S6= 0, then the microprocessor caused this bus cycle.

If S5= 0, then INTR interrupts are disabled
If S5= 1, then INTR is enabled

For Maximum mode processors only:

If S6= 1, then a co-processor or other DMA device caused this bus cycle.

If S5= 0, then the co-processor is an 8087
If S5= 1, then the co-processor is an 8089

Note:
When disassembly of 8087 instructions is enabled (see section 8.B, "X Key"), or when DMA cycles are present, the disassembler relies upon the above conventions to distinguish 8086/8088 cycles from all others.

D. POD CONNECTION ERROR WARNINGS

A "POD CONNECTION ERROR" warning is given by any of the PM 3632 microprocessor Pods if the Pod is not properly connected to the target microprocessor, or if power is not applied to the target.
The PM 8876 Pod is no exception, but this Pod also issues the warning for another reason.

If the DIP switch settings indicate that the microprocessor is running in Minimum mode, but the MIN/MAX pin of the target microprocessor indicates Maximum mode (or vice versa), a "POD CONNECTION ERROR" will be issued.
To correct this condition, the DIP switch settings must be changed, and the PM 3632 power must be cycled.

The 8087 and 8089 co-processors do not have a MIN/MAX pin, and the user may defeat the warning hardware to allow the Pod to be clipped directly to one of these co-processors.
To defeat this warning:
-open the Pod box and find jumper JP2, next to U42. Refer to Fig. 5.6 below.
-move the shorting jumper to short pin 2 (middle pin) to pin 3 (towards U49).
The shorting jumper is normally installed on pin 1 and pin 2.

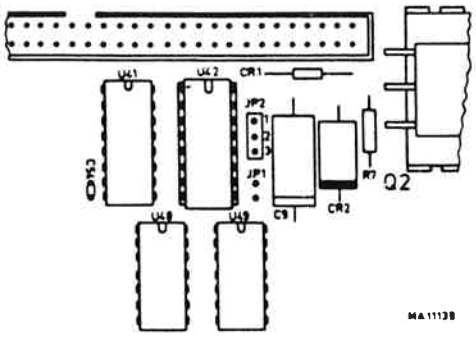


Fig. 5.6 *Jumper JP2 inside the PM 8876 Pod.*

3. MINIMUM PROCESSOR MODE (TRANSPARENT POD MODE ONLY)
(8086mn and 8088mn)

The 8086 and 8088 microprocessors operate in two modes, Minimum and Maximum. Processors operating in Minimum mode provide few indications of their internal operation; in particular, there is no indication of instruction queue activity outside the Minimum mode processor.
For Minimum mode processors, the PM 3632 offers only the Transparent Pod mode, which causes the PM 8876 Pod to transmit processor bus cycles to the PM 3632 data memory in the same order in which they occur.

Over-fetched instructions (those instructions pre-fetched but later discarded due to a jump, interrupt or other discontinuity in program flow) may trigger the analyzer in spite of the fact that these instructions were not executed.

Triggering on instructions which are occasionally over-fetched can usually be overcome by triggering on a later instruction in the same code path (one which is further downstream from a jump, call, return, etc., which is causing the over-fetch), or by using a more complicated trigger sequence to determine whether the instruction is actually executed, or not.

4. MAXIMUM PROCESSOR MODE WITH TRANSPARENT POD MODE

Because processors operating in Maximum mode provide queue status information, the PM 8876 Pod offers three "POD MODE" entries on the FORMAT setup screen when the Maximum processor mode has been selected (via the Pod DIP switch).
The first of the three modes, Transparent (8086T or 8088T), does not use the queue status information; this Pod mode causes the Pod to send processor bus cycles as they occur. Over-fetches are not stripped, and triggering on over-fetches may occur (same as Min-mode, see section 3).
If the over-fetches cause triggering problems, put the Pod in the Filtered mode.

5. MAXIMUM PROCESSOR MODE WITH FILTERED POD MODE

A. 8086F AND 8088F MODES

In the filtered modes (8086F or 8088F), the PM 8876 Pod maintains an instruction queue of its own, and transmits the instruction byte from the queue only when the queue status pins on the processor indicate that these bytes are actually used.
Over-fetched bytes are never sent to the PM 3632, and they cannot cause triggering.
Instruction bytes are delayed in the Pod until their actual execution, they will appear later in the memory relative to nearby data (non-instruction) bus cycles.
This slight delay of the instruction bytes has no effect upon the display of trace memory as disassembled code. The delay, and the absence of over-fetch, relative to transparent mode, can be seen only in the STATE data

In Filtered mode, the instruction queue is handled on a byte-by-byte basis. For the 8086, which pre-fetches words (two bytes) at a time, the Pod has the capabiity of repacking the executed instruction bytes into the original words, and (via a DIP switch on the Pod), the user can somewhat control the repacking of program bytes. The remainder of this section discusses the action of this switch, and applies only to the 8086F mode.

B. 8086F MODE, REPACKING INSTRUCTION BYTES (See also Section 7.C)

In the 8086F mode only, Switch 3 in the Down position causes the Pod to delay sending a lower byte of an instruction word until the disposition of the upper byte is known, or until a non-instruction data cycle occurs. The Pod will never allow a non-instruction bus cycle to enter the trace memory ahead of an executed instruction byte which may have caused the data cycle.
So, whenever possible, the Pod will repack a low-byte/high-byte pair of instruction bytes when Switch 3 is down. This repacking will not occur if one of the bytes is not executed, or if a non-instruction bus cycle occurs between the execution of the two bytes. Keeping Switch 3 down, uses the available trace memory much more efficiently.

In the Up position, Switch 3 commands the Pod, in Filtered mode, to transmit executed instruction bytes from its queue as soon as they are available.
Bytes will be repacked into words only if, due to some delay such as the transmission of data cycles, the Pod finds a low/high pair of instruction bytes has been executed and neither has been transmitted to the PM 3632. Thus, with Switch 3 up, repacking will only occur as required; the Pod makes no special effort to repack the instruction bytes.
The Up position is useful when the processor "hangs" after executing a WAIT or a HALT.
The Pod will empty itself of all executed instructions rather than keep the last byte (if it was a low byte), waiting for another instruction.

Switch 3 may be changed at any time, even while the Pod is gathering data; power does not need to be cycled, and the change of Pod operation takes place immediately.
With Switch 3 in the Up position, trace memory is less efficiently used, and the disassembly software may be unable to disassemble portions of the recorded data. In general, Switch 3 should be Down.

In the 8086F mode, when an instruction byte is transmitted separately from a companion byte in the same pre-fetched word, BHEX* and A0 modified to refer to the proper byte out of a split word.

6. MAXIMUM PROCESSOR MODE WITH JUMP POD MODE
(8086J and 8088J)

In the 8086J and 8088J modes, the PM 3632 records discontinuities in program flow due to jumps, calls, returns, interrupts, etc.
At each discontinuity, two entries are recorded in trace memory:
-the Source, and
-the Destination.

The Source is the address and the first byte of the instruction which caused the discontinuity, or was last executed before a hardware interrupt.

The Destination is the address and first byte of the instruction which was executed just after the discontinuity.
A special status bit (SRC) is high for the Source entry, and low for the destination entry.
Another status bit (ID*) is low for those destination entries which are caused by INTR hardware interrupts.

Switch 4 of the DIP switches allows the user to select between recording only discontinuities due to the INTR hardware interrupt (Down), or all discontinuities (Up).

The Jump mode is especially usefull for debugging runaway software or following the decision-making logic in a block of code.
In this mode, only the first bytes of the instructions on each side of a discontinuity are available to the disassembler. Therefore, only the mnemonic can be displayed by the disassembler, if that much. No operands or data cycles are available for display.

For some instructions, the first byte alone does not specify a mnemonic. For these instructions, a guess (indicated by a question mark) is made at the mnemonic, and only the displayed byte value and address are certain. By using the address value, the user can locate the actual instruction in an assembled code listing.

7. TRIGGERING

A. TRIGGERING SEQUENCE LIMITATIONS IN 62-BIT OPERATION

The basic width of the PM 3632 data path is 32 bits.
In order to accommodate 16-bit processors, the PM 3632 divides a processor-cycle into halves, and these halves are stored sequentially. One bit of each set of 32 bits marks which half is which, leaving 31 bits per half and a total of 62 bits to store information.

The basic triggering mechanism in the PM 3632 is also 32 bits wide and has up to 13 states. When only the upper 31 bits of information (the Status and Address fields) are used, all triggering capabilities are available as described in chapter 3.5, 3.6 and 3.7. However, it is often necessary to use the Binary and Data fields to trigger.
Special software allows the user to specify a single 62-bit trigger word.

In general, the software allows the user to be unconcerned with the triggering width of the machine; but there are some limitations.
Some complex sequences require too many states to be implemented in the 13-state sequence machine.
E.g., when the trigger words have something other than X's in their lower 31 bits, the Trigger Sequence "A+B+C+D" requires 16 states to represent the condition past the first half of the trigger word. This sequence is unavailable when Binary and Data fields (other than "Don't Cares") are specified.

User-Defined Sequence
Here the number of states needed for a given condition level can be calculated using these rules:

> A single word requires two states. If further words are "ORed" in, double the number of states for each additional "true" word (e.g., A as opposed to A*).
> If words are "ANDed" in, double for each additional "not" word (e.g.,A*).

E. g., the number of states required for a given condition level are:

Condition	No. of States
A	2
A + B	4
A + B + C*	4
A & B	2
A* & B*	4
A + B + C	8
A* & B* & C*	8

Number of states per trigger condition

Each level consists of two conditions; (refer also to Fig. 3.6).
-add the number of states required for each set of two conditions,
-multiply the resultant sum by the count for that level,
-sum at each level to obtain the total number of states.

The maximum number of states allowed is 13.

However, it is usually not worth the time to determine the number of states required by a particular sequence.
Simply enter the sequence on the TRIGGER SEQUENCE setup screen, and the PM 3632 trigger and sequence software will decide whether the sequence is too complex.
If it is, the PM 3632 will display an error message ("TRIGGER TOO COMPLEX") on the STATUS screen, just remove a word from a condition or reduce the count at a level, and try it again.

B. DATA QUALIFICATION

Due to the 32-bit nature of the PM 3632 capture and trigger circuitry, only the upper 31 bits (the default Status and Address fields) of a processor cycle may be used to qualify data storage.
Thus cycles may be qualified based on Address and access type, but not on the Data field.
Although the qualification decision is based on the first (upper) half of the cycle, the decision holds for the second (lower) half of the cycle.
I.e., whole 62-bit frames are either qualified or not qualified.

C. UNDESIRED TRIGGERING WITH PRE-FETCHING OR BYTE REPACKING

The pre-fetch mechanism of the 8086 or 8088 causes the microprocessor to fetch some bytes from code space which are subsequently discarded due to a jump, call or other discontinuity in program flow.
These fetched but unexpected instruction bytes are called over-fetches, and they present potential problems to those trying to debug code.
Typically, the user wants to trigger logic analyzers on executed instructions, and over-fetched instructions can cause false triggering when they are included in the triggering setup.

The Filtered Pod mode strips over-fetched code from the samples sent to the PM 3632, but the Filtered mode cannot be used for all applications (e.g., Minimum mode processors), and the 8086F mode presents some triggering complications due to instruction byte repacking.

This section suggests methods to overcome triggering problems created by over-fetching in the Transparent pod modes, or by repacking in the 8086F mode.

a. Over-fetch problems in the Transparent mode

For Minimum-mode processors, or for Maximum-mode processors being recorded using a Transparent pod mode, over-fetches will sometimes present a problem while trying to trigger the logic analyzer.
A few tricks may be used to trigger the analyzer when the instruction is actually executed rather than over-fetched.

Method 1:
(Maximum-mode only)
-Switch to a Filtered pod mode.

Method 2:
-If possible, set the trigger word to an instruction downstream from the over-fetched instruction, but in the same execution path.
To avoid false triggering, this downstream instruction must be far enough away from the cause of the over-fetching (a jump, call, return, software interrupt, or other interrupting instruction) that the over-fetching does not reach the downstream instruction.

Method 3:
-Trigger on a non-instruction data access unique to the instruction desired, or another instruction in the same code path.
Unexecuted instructions do not perform any non-instruction data accesses.

Method 4:
-Trigger on a sequence of instruction fetches and/or data accesses unique to the code path desired.

b. Triggering Problems Due to Instruction Byte Separation within a Word (8086 Processor only)

The processor object code comprises instructions quantized in units of bytes; that is, the smallest instruction is one byte long, and instructions range in size up to six bytes, with all sizes in between included.
The 8086 usually pre-fetches words, therefore in general one pre-fetch bus cycle may contain bytes belonging to two different instructions.
Even if the bytes belong to one instruction, the processor can be viewed as "using" the bytes at different times, not simultaneously.
If the 8086 pre-fetches a single byte or if (in the 8086F mode) the Pod sends the bytes of a pre-fetched word individually, the user may have trouble triggering on a particular instruction byte.

The 8086 will pre-fetch a single byte only when that byte is a high byte (i.e., has an odd address), and when that byte is the destination of a jump, return, or other discontinuity, included return from an interrupt service routine which executed between the low- and high bytes of a word.
If this odd byte is always accessed singly, the user can simply trigger at the odd address with BHE* set to 0.
If, however, this byte may also be pre-fetched as part of a word at an even address, Method 2 or Method 3 (below) must be used.

In the 8086F mode, the PM 8876 Pod can repack the individual instruction bytes of pre-fetched words into words.
The user can somewhat control the degree to which this repacking occurs via Switch 3 on the Pod.
Unfortunately, the settings of this switch cannot guarantee that repacking will never occur or always occurs.

Because the Pod alters bits A0 and BHE* according to which byte or bytes are sent to the PM 3632 in a given instruction record, and since the user cannot absolutely predict that a given pair of bytes will or will not be repacked, triggering on the address of a particular instruction may be difficult.

The following methods are recommended to overcome the problems created by pre-fetching and repacking uncertainties:

Method 1:
(for triggering on a low byte)
-Specify the address in the hexadecimal Address field, and place an "X" in the BHE* status bit.

Method 2:
(for triggering on a high byte)
-On the FORMAT setup screen, create a binary Address field duplicating the four least-significant address bits (A3--A0, Probe 35--32).
-Specify the main portion of the address in the hex field.
-Place "0" in the BHE* status bit of the trigger word.
-Place an "X" in A0 of the binary Address field.
Note that placing a "X" in A0 will cause a "?" to appear in the least significant nibble of the hex Address field. The values of A3--A1 can be determined by examining the binary Address field.
When creating the new field on the FORMAT setup screen, note that the "Sense" of the field should never be "Inverted" (INV).

Method 3:
(for triggering on a high byte)
-Using two trigger words (for example, A and B), enter the even address of the word containing the high byte in A, and the odd address of the byte itself in B.
-Place "0" in the BHE* bit of both words.
-Trigger on "A or B" or similar sequence.

8. DISPLAY

A. GENERAL

With the PM 8876 Pod in the Transparent mode, the State display shows all instruction fetches and data cycles in the same order in which they occured on the bus.
In the Filtered mode, the order of cycles in the memory will not match the actual order of cycles on the processor bus (see Section 5, "Filtered Mode"), and any unused fetches (fetches following an instruction causing a program discontinuity) are disqualified by the pod and not stored in the memory.

The Disassembly display groups these program fetches and data cycles into assembly language instructions. Regardless of whether or not the Pod is filtering unused fetches, these unused fetches are not displayed on the Disassembly screen. The current pod mode is shown in a reversed field at the top of the Disassembly screen.

The formatting and display of data is described generally for the PM 3632 in chapters 3 (SET UP) and 4 (DATA DISPLAYS).
Further details of data display when using 16-bit microprocessor pods, including typical State and Disassembly display screens, keyboard functions and display formats, follow.

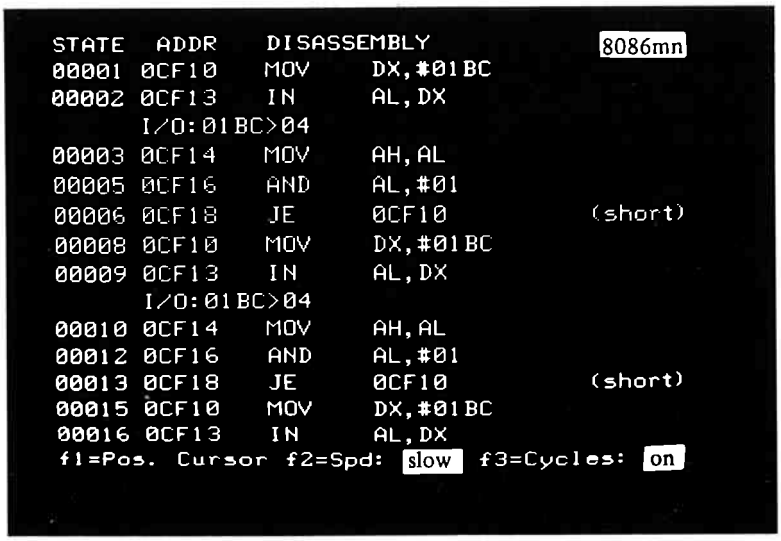


Fig. 5.7 *Disassembly Display (Transparent and Filtered Modes)*

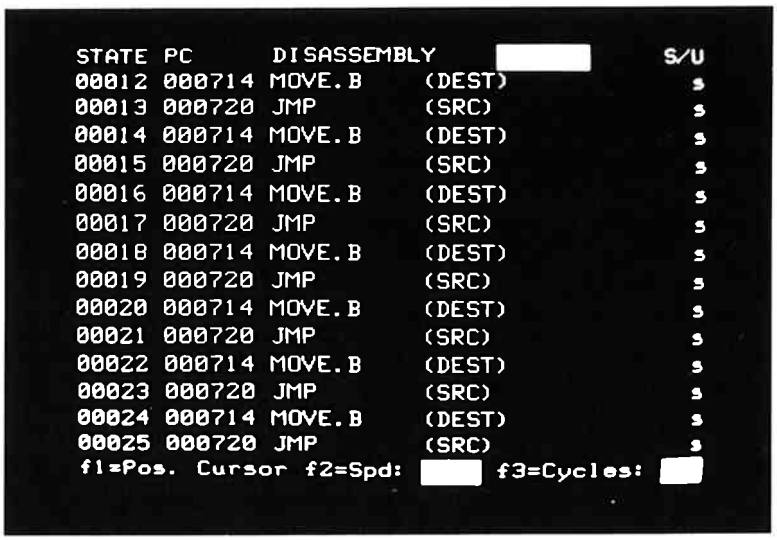


Fig. 5.8 *Disassembly Display (Jump Mode)*

B. KEY FUNCTIONS ON THE DISASSEMBLY DISPLAY SCREEN

f1 Key (Position Cursor):
To move the cursor directly to any location in the memory:
-depress the f1 key,
-enter the state number you wish to display
-and depress f1 again.
Negative state numbers correspond to cycles before the trigger event, positive state numbers correspond to cycles after the trigger.
If f1 is inadvertently depressed, depress it again to leave the cursor at its current location.

Up/Down Arrow Keys (Scroll through the memory):
To move through the memory backward or forward, use the Up and Down Arrow keys.

f2 Key (Scroll Speed):
To scroll slowly through the memory (one instruction at a time), use the f2 key to set the scroll speed to Slow.
To scroll faster, toggle the f2 key to set the scroll speed to Fast.

f3 Key (Data Cycles On/Off):
To view the disassembled instructions without their associated data cycles, depress the f3 key. This gives a display very similar to an actual code listing and makes it easier to locate a particular section of code.
To turn the data cycles back on, toggle the f3 key.

f4 Key (Print Screen):
To print a hardcopy report of the Disassembly screen, depress the f4 key.
There is no on-screen prompt for this function.
Note that the RS-232C option must be installed; this is included in the ROM Emulator Module, PM 8880/00.

DISAM Key (Display Trigger Condition):
To display the trigger event, depress the DISAM key once to enter the the Disassembly screen, and again to display the trigger event.

X Key (8087 Disassmbly--Maximum processor mode only):
To alternately enable or disable the display of "ESC" instructions as 8087 mnemonics, depress the X key.

C. DISASSEMBLY DISPLAY FORMATS

a. Instruction Display

As with 8-bit microprocessor pod disassembly, each instruction displayed contains a state number corresponding to the instruction position relative to the trigger event, the value of the Program Counter when the instruction was fetched (PC), and the mnemonic and operands for the instruction itself.

b. Data Cycles Display (including 8087 data cycles)

Data cycles are displayed on lines following the instruction that caused them. Display of these cycles may be turned on or off by toggling the f3 key.

Each data cycle contains an indication of its segment (ES:, DS:, CS:, SS:, or I/O:), an address, an indication of whether data was read from (>) or written to (<) the address, and the data itself.
Each address consists of five hexadecimal characters (20 bits), while data may be a byte (2 characters), or a word (4 characters) for non-8087 instructions.

Although the bytes of a word may have been accessed in two separate bus cycles (e.g., an 8086 accessing a word at an odd address or an 8088), the two bytes will be combined into a single word for display.

Some instructions (such as calls, returns, etc.) have some of their data-cycles labelled to identify the Instruction Pointer, "(IP)", and CS Register "(CS)".
These labels may appear more than once in the same set of bus cycles, since often the current value is written to the stack and a new value is then read from memory.

The data cycles of repeated string instructions will be displayed, two per line, on up to 13 lines.
To view those cycles beyond these 26 bytes or words, the user must search through the State display data.

The data cycles of 8087 instructions may be as long as 94 bytes. These will be shown on multiple lines, as necessary. The bytes of each separate floating point or integer value will be grouped under a separate address. The 14 bytes comprising the internal status of the 8087, when read or written, will be grouped under a single address. The address will be that of the lowest addressed byte, and that low byte will be the rightmost of the group.

If some or all of the data cycles of an 8087 instruction are missing from the trace memory (possible because they occured much further downstream), their place will be denoted by "XX" in the data.

The 8087 will access only the data segment of memory. If an 8087 instruction is preceded by a segment overriding prefix, the 8086/8088 will read data from some segment other than DS:. The 8087 then accesses the remaining data bytes in DS:. In this situation, the data cycles of the 8087 instruction will blink to warn of the mixed segment access by the processor/co-processor combination.

c. Interrupts

Interrupts will be labelled as "EXTERNAL" or "SOFTWARE" (or, in some cases, even more specifically, such as "DIVIDE OVERFLOW", etc.), and their type (vector number) will be displayed.
Additionally, the data cycles will be labelled during the stacking of the instruction pointer "(IP)", the code segment register "(CS)", and the flag register,"(F)". The new instruction pointer and code segment register retrieved from the vector area will also be labelled.

d. Question marks

Occasionally (often just before interrupts) when operating the Pod in a Transparent mode, some instructions will be labelled with a question mark. In these instances, the disassembler is unable to determine if these instructions actually were executed.

e. DISASSEMBLY MESSAGES

Accurate disassembly of the 8086 or 8088 bus cycles requires extensive pattern matching and decision making. For Transparent pod modes, identifying those code segment bytes which are the first bytes of instructions is a difficult task, requiring the disassembler to make initial guesses concerning the first bytes of instructions and the locating of data cycles relating to a given instruction.
These guesses are modified until the trace memory is disassembled without any discrepancies in fitting known patterns to each instruction.

The Filtered modes are simpler to disassemble, due to the presence of "first-byte" status bits on instruction bytes, but locating the non-instruction cycles associated with certain instructions still requires iterative matching of patterns throughout the memory

The only recording modes which do not require extensive effort to disassemble are the Jump modes.

Occasionally, the trace memory may contain a singularity (an abrupt, small irregularity), through which disassembly cannot pass without a pattern-discrepancy.
Such a singularity can arise from the use of data qualification, or due to the resetting of the microprocessor while recording.
The disassembler will recover from these singularities in several ways, depending mostly upon how large a piece of trace memory was successfully pattern-matched just preceding the singularity, and whether or not there are signs that the processor was reset.

If a reset occurred, the disassembler will display a line with "RESET" in the Address field, and then the pattern-matching will resume past the singularity.
If the singularity is not due to reset, and a significant number of instructions matched their specific patterns before the singularity, the disassembler will display "UNABLE TO DISASSEMBLE XXX CYCLES", where XXX is the number of confusing cycles.
Disassembly will proceed beyond the singularity.

If too few instructions are successfully matched before a singularity disrupts the disassembly, the disassembler will discontinue its effort to completely disassemble the trace memory, and will display the message: "CAN'T DISASSEMBLE--CS READS USED AS OPCODES".
From that message forward, the mnemonic that each code space read would represent if it where the first byte of an instruction is displayed.
These mnemonics are preceded by a question mark to indicate that the disassembler could make no sense of the recorded data.

6 DESCRIPTION OF THE OPTIONS

6.1 GENERAL

The following options (except the PM 8864 Rom Emulator Pod) must be located inside the PM 3632 Analyzer.
The main p.c.board inside the Analyzer has been provided with three p.c. board connector slots for mounting these options.
For Installation Instructions refer to Chapter 7.
The PM 8880/00 Rom Emulator Module functions can be found under PM 8864 and PM 8880/20.

6.2 ROM EMULATOR POD PM 8864

6.2.1 INTRODUCTION

The Rom Emulator Pod, which is part of the Rom Emulator Module PM 8880/00, enables the PM 3632 to emulate one or more 27xx-series Eproms, giving it a powerful tool for debugging machine-code in microprocessor-based systems.
The machine-code as present in the B reference memory can be downloaded to the emulator and then patched as required.
The ROM Emulator Module consists of two assemblies:

- -ROM Emulator Pod PM 8864
- -RS-232C Communication Card PM 8880/20 (an internal card)

With one Emulator Pod, up to 16 Kbytes of memory may be emulated and configured as four 2716s, four 2732s, two 2764s, or one 27128. With a second Emulator Pod, twice the memory can be emulated. The PM 3632 accommodates no more than two ROM Emulator Pods.
The PM 8880/20 is always required with ROM emulation, even if no RS-232C communication is applied.

6.2.2 CONNECTION TO THE PM 3632

If one Emulation Pod is used, connect the Rom Emulator cable from the PM 3632 to the IN connector on the Emulation unit. If two Emulation Pods are used, connect the first one as described above, and connect the IN connector of the second Pod to the OUT connector on the first Pod.

6.2.3 SET-UP AND EDITING

To access the ROM Emulator function, depress the S.FUNC key on the PM 3632 front panel, then select one of four screens via the keypad, as shown below:

Key	Function
3	RS-232C Port Configuration
4	ROM Emulator Transfers
5	ROM Emulator Configuration
6	ROM Emulator Editor

RS-232C Configuration

RS-232C configuration is used to configure the serial port to download or upload information to or from the ROM Emulator. It allows the user to select the number of bits per character, the parity, and whether or not the port should recognize CLEAR TO SEND ("CTS"), whether it should add linefeeds to carriage turns, and whether it should delay after transmitting a character and/or allow a different delay for carriage return for devices which are slow to receive characters.

ROM Emulator Transfer

The ROM Emulator Transfer screen is used to upload or download data to or from the ROM Emulator, and allows the user to select the following:

- -which Prom to download to or upload from;
- -the lowest address and highest address to be recognized;
- -the transfer format (currently available are Intel hex, Tek hex, S Records (Motorola), and MOS Technology.
- -a transfer type, either copy or verify, (for verifying data already in ROMs in case previous edits have been forgotten); and
- -transfer direction (to or from the PM 3632 RS-232C-port).

ROM areas must be enabled before being downloaded to; this is accomplished via the Configuration screen as described below.

There are two Intel transfer formats and three Motorola transfer formats; only one of each appears on the Transfer screen. In each case, the transfer formats are upward compatible; i.e., Intel has both 8-bit and 16-bit formats. The 8-bit format is a subset of the 16-bit format, and the unit will allow the 16-bit format to be downloaded in any case. During upload it will check the address size; if it is 20 bits, it will upload using Intel 16-bit format, and if it is 16 bits, it will upload using Intel 8-bit format.

Similar decisions are made on the Motorola format. The Motorola format allows different address lengths to be downloaded (16-, 24-, or 32-bit). The PM 3632 will accept any of the three on download, and will check the address with selected via the configuration screen to determine which format to use to upload.

ROM Emulator Configuration

The ROM Emulator Configuration screen enables the user to configure the way in which the ROM Emulator appears to the hardware, as well as to the user, when editing or downloading. The user may select:

- -the numeric base to be used in editing (octal or hexadecimal);
- -the address and data widths in bits (address widths may be from 11 to 24 bits, and data bits from 8 to 32 bits);
- -the addressing mode (either one address per byte or one address per word, where a word is the selected data width); and
- -the device type for a given ROM pod;

All of the above are selectable for each of the two ROM pods, if two ROM pods are installed. An exception is when the user selects 32-bit data width, in which case the two ROM Emulator Pods are necessary to provide 32 bits of data. If the device selected is 27128, 32 bits are not available, and, in fact, two ROM pods are required to emulate 16 bits. If a nonstandard data width is entered (other than 8, 16 or 32 bits), then it is rounded up to the nearest above value. Data widths over 32 bits are not allowed.

The Configuration screen sets up fields which enable the user to set base addresses for the Roms being emulated, making editing and downloading convenient. For example, when the Rom Emulator is emulating four 2716s, one Rom may have a base address of 1000 hex, etc.; this is achieved by positioning the cursor in the appropriate fields, on the Configuration screen, entering "0" in the first field, "800" in the next field, etc. Base addresses must be set to enable areas of ROM; if an area is not enabled, it cannot be downloaded to or edited.

ROM Emulator Editor

The ROM Emulator Edit screen enables the user to edit data in the ROM. There are essentially two alterable fields in this display, one for the address and the other for data. The user, using the UP and DOWN arrow keys, scrolls to the desired address, or enters in the lefthand field a new address for editing. To edit the data, position the cursor in the data field (the righthand field) and enter the new data via the keypad. (The new data will be displayed as soon as the cursor exits the field, as is the case with the address field). While editing, the user can view six locations above and six locations below the currently addressed field, and so get an idea of where he is in his ROM, what he has done, and what he needs yet to do.

The following functions are available in the editor and are accessed by depressing the appropriate function key:

f1 Restores the field being edited to the value in it before editing began (available only until cursor exit field).

f2 Toggles the ROM pod number to select pod in multibyte applications.

f3 Causes checksum to be computed:
(1) In any address field, enter the low address for the checksum range.

(2) Cursor to the data field, then back to the address field.

(3) Enter high address of checksum range.

(4) Depress f3.

f4 Fills memory with desired constant data:

(1) In any arbitrary address, enter low address of fill range.

(2) Cursor to data field.

(3) Enter fill range data

(4) Cursor back to address field and enter upper address of fill range.

(5) Depress f4.

NOTE: While editing or downloading or uploading from the ROM Emulator, it is not accessible as ROMs. Therefore, it will probably be necessary to reset the target after any of these operations.

6.2.4 HARDWARE CONSIDERATIONS

The ROM Emulator hardware is capable of detecting whether a ROM socket has been plugged in backwards, has not been plugged in, or has been plugged into a system with no power. The software will make checks when the user exits the Edit screen. These checks, if they run into an inconsistency, will flag an error. Selection of ROMs to be used is accomplished on the Configuration screen. If the base address is set with "Xs", it is treated as unused.

If a parity error occurs during transfers, a beep will be generated. If an overrun or framing error occurs, or if an illegal character is encountered, then transfer will immediately stop. Transfer will also be stopped by pushing the STOP key. On download, a byte is entered into the ROM Emulator if the address of that byte is between the lower and upper address bounds entered on the transfer screen and is also being emulated, as defined by the blocks of one of the address bases determined by the length of the device being emulated (either 2 Kbytes up to 16 Kbytes) and by the base address of the given ROMs.

6.2.5 ERROR CODES

Error code	Description
1	Checksum error
2	Nonhex character
3	Invalid character
4	Verify fail
16	Overrun error *)
32	Framing error *)
64	Break detect *)

*) Combination of these three errors may be shown as the sum of their error codes.

6.3 ROM EMULATOR MODULE PM 8880/00

This type number exists of:
-Rom Emulator Pod PM 8864
-RS-232C Communication Card PM 8880/20

For further details refer to the relative chapters.

6.4 RS-232C COMMUNICATION CARD PM 8880/20

6.4.1 GENERAL

This card is used for:
-Control of the Rom Emulator Pod PM 8864
-I/O Interface for peripheral equipment, such as a printer, or a data recorder.

6.4.2 RS-232C OPERATING EXAMPLES AND CONNECTION DETAILS

Introduction
The PM 3632 RS-232C Interface functions as a "DTE" device.

There are two possible handshake methods of controlling the RS-232C data-stream to and from the PM 3632.
1-Using the RTS and CTS lines.
2-Using the DC1 and DC3 (XON and XOFF) of the ASCII code.

The following signals are available on the RS-232C "DATA INTERFACE" connector at the rear panel of the PM 3632.

Pin no.	RS-232C Signal name	PM 3632 Input	PM 3632 Output
1	Frame ground	x	x
2	TXD		x
3	RXD	x	
4	RTS		x
5	CTS	x	
7	Signal ground	x	x

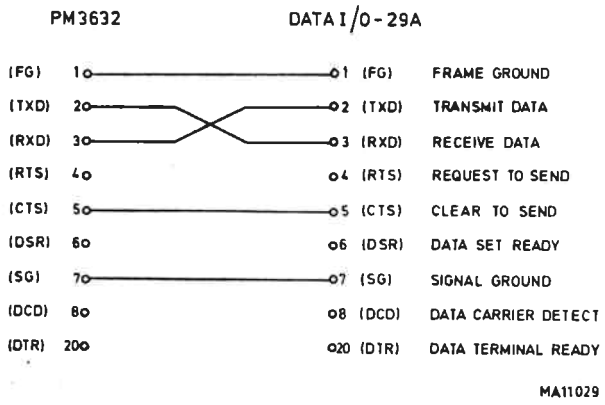


Fig. 6.1 The RS-232C cable between the PM 3632 and the Prom-Programmer.

In this example a 2716 is assumed as Prom to be programmed.
Prom connection 'A' of the Prom Emulator Pod is connected to the Prom-socket of the target system.
Where memory-addresses, -offsets, or blocksizes are mentioned, 4-digit hexadecimal values are meant (max. FFFFH).

PREPARATION

-Connect the RS-232C cable.

The following settings apply to both the Upload- and the Download procedures.
- PM 3623
- Set the RS-232C Port Configuration-, Rom Emulator Configuration- and the Rom Emulator menu according to Fig. 6.2--4.

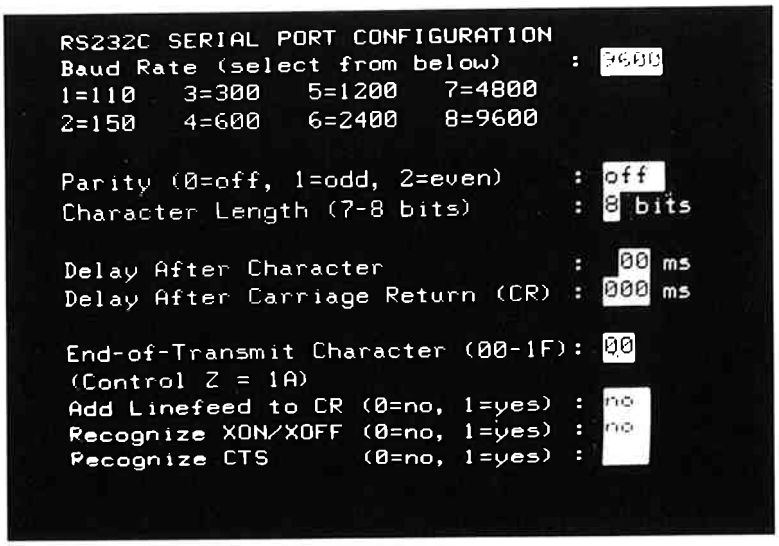


Fig. 6.2 *RS-232C Port Configuration Menu*

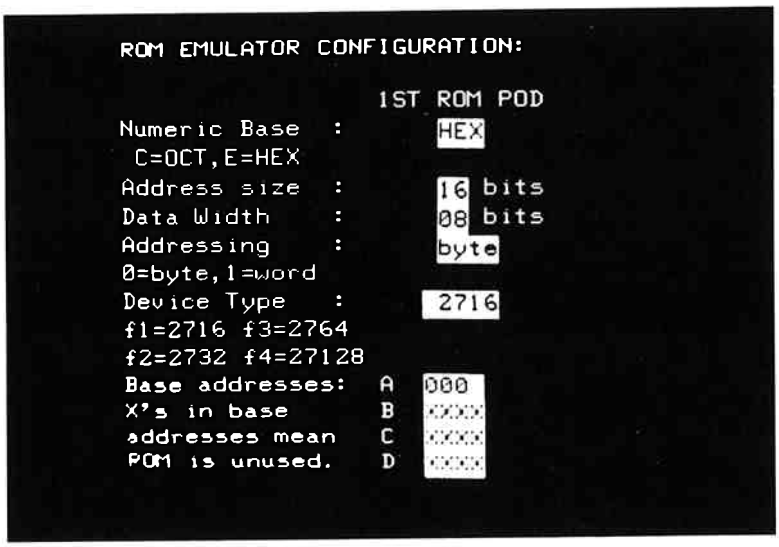


Fig. 6.3 *Rom Emulator Configuration Menu*

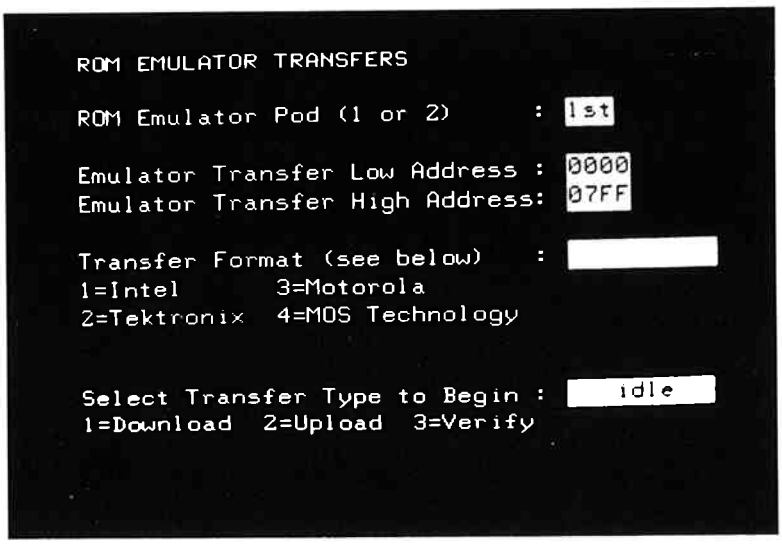


Fig. 6.4 *Rom Emulator Transfer Menu*

UPLOAD

(Data-transfer from the PM 3632 to the Prom-Programmer)

-Data is assumed to be in the ROM Emulator Pod.

-Set the PM 3632 according to the three menus as detailed under PREPARATION.

-Prom-Programmer settings:
    -Set transfer-format to Intel-Hex
     Press: <SELECT>; 83 ; <START>; <START>
    -Input from Port:
        -Press: <COPY>; <PORT>; <RAM>
            (if required PORT can be followed by an address-offset, and
            blocksize; RAM may be followed by a start-address).

-Prom-Programmer: Press <START>

-PM 3632:
    Select the Rom Emulator Transfers Menu. Cursor in 'idle' field.
    Press key 2 twice (Upload starts).

-Wait until the Prom-Programmer shows: INPUT DONE [checksum]

-Programm the PROM as follows:
    -Insert the PROM (socket #0)
    -Press: <COPY>; <RAM>; <DEVICE>; <START>
    -Press: 19 23 (Intel 2716 family-name and pin-out)
    -Press: <START>
    -Wait until the Prom-Programmer shows the correct checksum.

DOWNLOAD

(Data-transfer from the Prom-Programmer to the PM 3632)

-Set the PM 3632 according to the three menus as detailed under PREPARATION.

-Prom-Programmer:

-Set Transfer-format to Intel-Hex
Press: <SELECT>; 83 ; <START>; <START>.

-To load the PROM-contents into the Prom-Programmer:

-Insert the PROM
Press: <COPY>; <DEVICE>; <RAM>; <START>
Press: 19 23 (Intel 2716 family-name and pin-out)
Press: <START>

-Set: Output to Port
Press: <COPY>; <RAM>; <PORT>
Wenn downloading to Prom connection B, C, or D also specify:
Startaddress and Blocksize (prom-boundaries) and,
PORT-destignation address
Example: For connection A: 0000
B: 0800
C: 1000
D: 1800

-PM 3632:

-Select ROM Emulator Transfers menu. Cursor in 'idle' field.
Press key 1 twice
Now the PM 3632 is waiting for the Prom-Programmer to send data.

-Prom-Programmer: Press START

-Wait until the Prom-Programmer shows the message: OUTPUT DONE [checksum].
The PM 3632 beeps.
Now the data is in the ROM Emulator Pod.

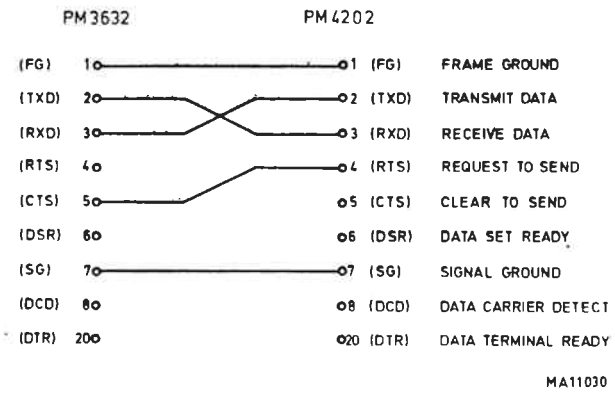


Fig. 6.5 *The RS-232C cable between the PM 3632 and the PM 4202.*

The following RS-232C Configuration applies to both the Upload- and Download modes.

Connect the cable between the PM 3632 and the PM 4202.
Check that the correct tape-casette is present in the PM 4202.

Note:
Upload- and Download-activity is controlled with the Saved B Memory Directory or the Setup File Directory on the PM 3632-display. The cursor position must be in the Action column.
However, data-transfer is only executed from or to the B reference memory or the instrument setting itself. There is no RS-232C data-transfer directly to or from the Saved B memory or the set-up files.

PREPARATION

-PM 3632:
-Set the RS-232C Port Configuration menu. Refer to Figure 6.2.

-PM 4202:
Set the switches at the back of the PM 4202 according to the following table.

Description	Set to:
Keys	Enable
Keys	Remote
Block length	1024
CRC Check	No
Auto rewind	Yes
Transparant	Yes
RS-232C	V24
Parity	Even
Word	8 bits
Stop bit	1
Parity check	Disable
Baud rate	9600

-The PM 4202 is used in the local control mode.

UPLOAD
(Transfers the actual PM 3632 setting or the B memory data to the recorder)

-Set the PM 3632 and the PM 4202 as detailed under PREPARATION.

-PM 3632
Select the SET-UP FILE DIRECTORY if the instrument setting must be stored, or the
SAVED B MEMORY DIRECTORY screen if the B Memory contents must be stored.
Set the cursor in the ACTION column.

-PM 4202: Press <WRITE> (tape positioning).

-PM 3632: Press f3 twice.
The tape moves.
The screen shows 'UPLOADING', until the original screen-text is restored.

-PM 4202: Press <WRITE> again to complete the data storage.
The END OF DATA lamp is on.
Press <STAND-BY>.

Data is now stored on tape.

DOWNLOAD
(Transfers recorded data into the PM 3632)

-Set the PM 3632 and the PM 4202 as detailed under PREPARATION.

-PM 3632
Select the SET-UP FILE DIRECTORY if a setting must be loaded into the instrument,
or the SAVED B MEMORY DIRECTORY screen if the B Memory must be loaded.
Set the cursor in the ACTION column.
Press f4 twice.
The PM 3632 screen shows 'DOWNLOADING'.

-PM 4202: Press <READ> (tape moves)
Data is now entering the PM 3632.

After completion the PM 4202 indicates END OF DATA, and goes to the STAND-BY mode.

EPSON-80 PRINTER

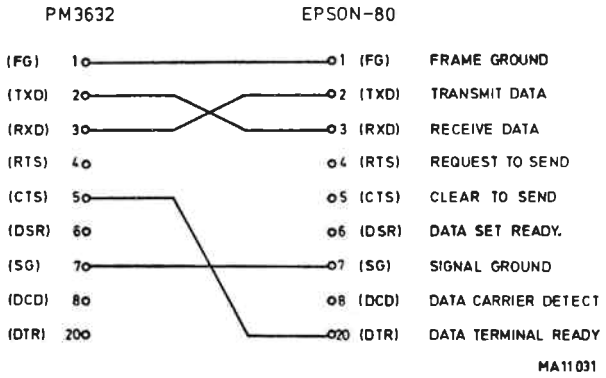


Fig. 6.6 *The RS-232C cable between the PM 3632 and the printer.*

-PM 3632:
-Set the RS-232C Port Configuration. Refer to Figure 6.2.

Various print-outs are possible. Refer to the following list.

Print-out	Select display	Action
State list (screen)	State list	Press f4
Disa list (screen)	Disa list	Press f4
Auto sequence results	Auto sequence results	Press f4
ROM Emul. data h)	ROM Emul. transfers	Press key 2 twice
Set-up h)*)	Set-up storage	Press f3 twice
B-Memory h)*)	B Memory storage	Press f3 twice

h) Hexdump

*) Only the actual set-up of the instrument or only the B Memory reference-data are printed, not the saved set-up files, nor the saved B memory data files.

6.5 DISASSEMBLY ROM BOARD PM 8080/30

This board features conversion of the machine code to the assembly-language mnemonics, for the most current microprocessors.
This board must be provided with a specific disassembly Prom for each microprocessor model. These Proms are included in delivery of a microprocessor Pod.
Up to eight disassembly Proms for eight different microprocessors can be located on this unit.

Prom location:
Disassembly Proms type 2732 and type 2764 may be located in any socket (U1--8) on this unit.
Disassembly Proms type 27128 may only be located in sockets U5--8.

For building-in refer to chapter 7, for the operation refer to chapter 5.4.

6.6 PM 8880/40 SET-UP MEMORY
PM 8880/50 SET-UP AND DATA MEMORY

6.6.1 INTRODUCTION

The Set-up and Data Memory Option has all the basic capabilities of the Set-up Memory Option, plus enhanced data memory capabilities as well. With the additon of either option, the PM 36.8 logic analyzer becomes an even more effective instrument for data analysis, portable field service work, and production test.

N O T E

IN THESE OPTIONS THE SET-UP AND DATA FILES CAN HAVE A 'PROTECTED' STATUS.

TO PREVENT ACCESS TO PROTECTED FILES A SECURITY CODE IS USED AS A PASSWORD.

BE SURE NEVER TO FORGET THIS SECURITY CODE OTHERWISE NO FURTHER ACCESS TO THESE FILES OR TO THESE MEMORY SEGMENTS IS POSSIBLE.

6.6.2 SET-UP MEMORY

This unit saves eight complete machine set-ups (trigger words, timing line labels, format specifications, etc.) in non-volatile memory. These set-ups are retained when power is turned off.

This storage of set-up files permits rapid, convenient paging between different analysis methods for any given piece of captured data (i.e., paging between different sets of timing lines with alternate labels and positions on the display screen.)

Similarly, without re-entering any labeling or triggering conditions, the user can switch from a 32-channel, state, data-qualified mode to a 4-channel, 100-MHz mode immediately, and have all of the data capture parameters already defined. Also, complex set-up data need not be lost when there are interruptions and the user needs to be away from the logic analyzer for long periods of time.

6.6.3 SET-UP AND DATA MEMORY (B-MEMORY)

This unit, in addition to saving eight complete machine set-ups, expands the PM 3632's capabillities further by adding a B (reference) Memory. The B Memory is the same size as the machine's A (data record) Memory (1,000 sampls deep at 32 channels wide, and 8,000 sampls deep at 4 channels wide).
With the B Memory in this option, Compare and Search functions have been added to the PM 36.8 to facilitate more extensive data analysis. In addition, B Memory may be edited to allow the Search and Compare functions to be more selective.
The B Memory may also be saved in non-volatile memory on this option.

6.6.4 INSTALLATION

Both the Set-up and the Set-up and Data memory options are each contained on a single option card, which is field-installable. Refer to chapter 7.

6.6.5 OVERALL OPERATION

The Set-up Memory function of storing set-ups is operated via the Set-up Storage screen.
The Set-up/Data Memory Option uses the same Set-up Storage screen, plus four other screens: B Memory Storage, Compare, Search, and Edit B Memory.

To access the Set-up Memory functions, depress the Special Function key, then depress the key on the keypad which corresponds to the function:

Key	Function
7	Set-up Storage
8	B Memory Storage *)
9	Compare *)
A	Search *)
B	B Memory Edit *)

*) In PM 8880/50 only.

6.6.6 SETUP STORAGE (See Figures 6.7a--c)

The Set-up Storage screen is shown in three following figures, with three different cursor positions.
Figure 6.7a shows the screen when the user has positioned the cursor in the Action field.
Figure 6.7b shows it with the cursor in the Name field.
Figure 6.7c shows it with the cursor in the Status field.
User activities via these three screens are detailed in Sections a, b, and c below.

On these screens, the Mode column indicates the set-up file mode, i.e., 8085, Z80, LOGIC4, etc. The correct pod must be connected to the PM 3632 before recalling a set-up file or a Pod Conflict error will occur.

In the Set-up column, an asterisk to the left of the file number indicates the current set-up file in use (last file accessed). An "M" to the right of the file number indicates that the set-ups currently in the PM 3632 have been modified and differ from the values in the file.

A. Saving Set-ups (Figure 6.7a)

Up to eight PM 3632 set-up files can be saved. A set-up file contains all set-up parameters selected by the user (including those of the RS-232C Communications Card and the ROM Emulator), except for search words.

To save a set-up file, put the cursor to its columnn field and depress the f1 key (SAVE set-ups), then depress f1 again (to verify the action).

To recall a set-up file, put the cursor to its action column and depress the f2 key (RECALL set-ups), then depress f2 again (to verify the action). The current set-ups will be replaced by the set-ups recalled from the file selected.

In the Set-up column, an asterisk to the left of the file number indicates the current set-up file in use (last file accessed). An "M" to the right of the file number indicates that the set-ups currently in the PM 3632 have been modified and differ from the values in the file.

If the RS-232C Communication Card or the ROM Emulator Module has been installed in the PM 3632, then machine set-ups may also be uploaded and downloaded via this screen.
To upload or download set-ups, put the cursor to the selected Action field and depress the f3 key ("UPLOAD 8") or the f4 key ("DOWNLOAD 8"). Set-ups are uploaded to or downloaded from machine memory rather than the files themselves, so the location of the cursor in the action column is unimportant. Downloaded set-ups may then be saved in a set-up file.

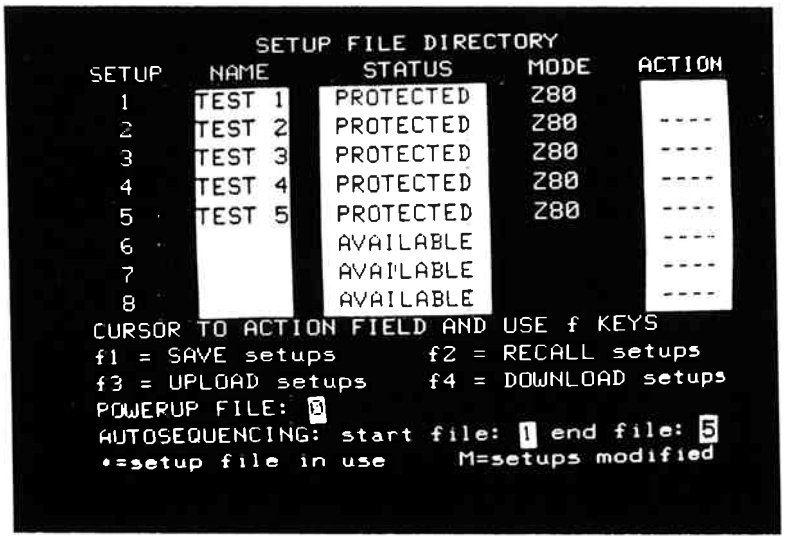


Fig. 6.7a *Set-up Storage Screen (cursor in Action field)*

B. File Names (Figure 6.7b)

Set-up files can be assigned names of up to six characters, before saving the file.
To enter a set-up file name, cursor to each space in the Name column and enter one character at a time, using the f1 and f2 keys to alphabetically advance or retreat characters, until the desired character is displayed in each space. The f3 key (clear field) may be used to clear the entire name field.

To change a set-up file name, edit the name field one character at a time, using the f1 and f2 keys, then save the file again. If a file name is changed without the file being resaved, a warning message will be issued if an attempt is made to exit the screen.

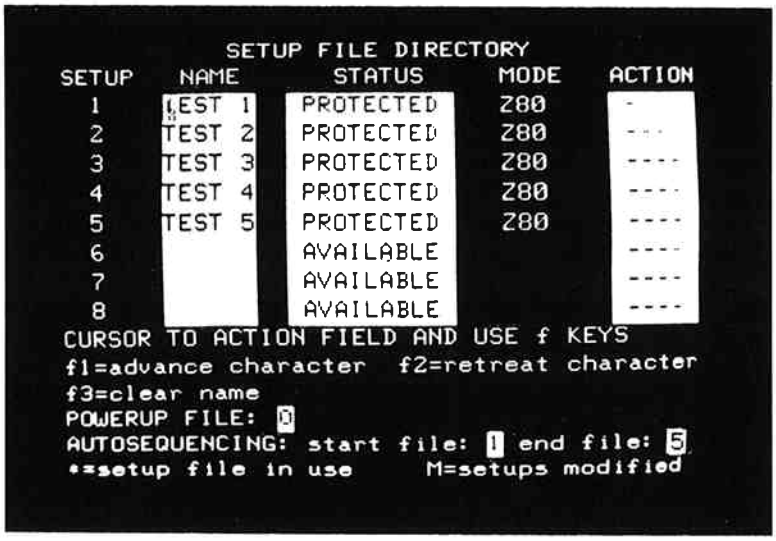


Fig. 6.7b *Set-up Storage Screen (cursor in Name field)*

C. Status (Protected, Unprotected, Available) (See Figure 6.7c)

Set-up files normally have a status of "Unprotected," but may also be "Protected."
To protect a set-up file, cursor to the Status field, depress the f3 key (protected), then save the file.
When the file is saved, a security code (password) will be requested; this is a 2-digit hexadecimal number which is entered on the keypad.
If more than two keys are depressed, only the last two are used.
The security code will not be displayed on the screen. This security code will be required to write over the file in the future, and it is strongly recommended that it be written down and stored for future use.

To change a set-up file from 'Protected' to 'Unprotected', cursor to the Status field, depress the f2 key, and save the file, using the correct security code.

To erase a set-up file, cursor to the Status field; depress the f1 key to change its status to 'Available', and save the file.

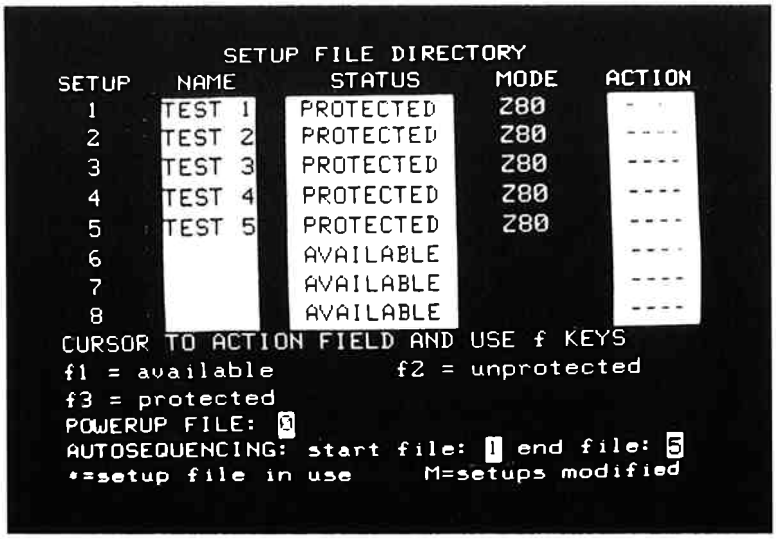


Fig. 6.7c *Set-up Storage Screen (cursor in Status field)*

D. Power-up Field

To designate a power-up set-up file, cursor to the Power-up field and enter the set-up file number; this set-up file will then be automatically recalled upon powerup.
To disable the power-up set-up, cursor to the Power-up field and enter 0.

E. Autosequencing Start and End (PM 8880/50 only)

The autosequencing start and end file fields apply only to the PM 8880/50 option. These fields select the set-up files to be used in autosequencing, a method of automatically running up to eight different tests a preset number of times. See section c, Autosequencing, for operating details.

6.6.7 B MEMORY STORAGE (PM 8880/50 only) See Figures 6.8a--c.

Data captured by the PM 3632 can be copied to the B Memory to be used as reference data for Compare operations. If non-volatile storage is wanted, this B Memory can be saved in a B Memory file.

The user has the option of configuring B Memory storage into one full-sized 4000-byte segment, two 2000-byte segments, four 1000-byte segments, or eight 500-byte segments. This feature permits storage of up to eight reference memories if the user decides (as in many cases) that only a portion of the trace buffer needs to be used for a Compare.

Note the distinction between B Memory and a B Memory file; the machine contains only one B Memory, but may have up to eight saved B Memory files.

The B memory Storage screen is shown in three figures in this section.
Figure 6.8a shows the screen when the user has positioned the cursor in the Action field.
Figure 6.8b shows it with the cursor in the Name field.
Figure 6.8c shows it with the cursor in the Status field.
User activities via these three screens are detailed in Sections 2a-e below.

The width of the stored data (32, 16, 8, or 4 channels) is shown for each file. The selected word width of the PM 3632 must match the width of the B memory file or an error will occur on recall.

As with the Set-up Storage screen, an asterisk to the left of the file number indicates that the current B Memory file in use (last file accessed).
An "M" to the right of the file number indicates that B Memory currently in the PM 36.8, differs from the file indicated by the asterisk.

A. B memory Configuration (See Figure 6.8a)

To select the configuration for saved B Memory, cursor to the B Memory Configuration field and enter 1, 2, 4 or 8 to specify the number of memories. Changing the configuration will change the size of the B Memory segments. As soon as B Memory is saved in a B Memory file, the B Memory directory is automatically updated to show the new number of files available.

For example, Figure 6.8a shows that there are eight B memory files available for use; changing the configuration to one would set the B Memory size to a 4000-byte memory. The B Memory Storage screen, however, would still show the eight files saved in nonvolatile memory, until a Save action is executed. At that time, the B Memory Storage screen would be updated to show only one B Memory file.

B. Copying Data (See Figure 6.8a)

To copy captured data in A Memory to B Memory, depress the "X" key.
If saved B Memory is configured to any size except one, start and end adresses for the copy will be requested.

If B Memory is configured to one, the entire A memory will be copied.
If there is insufficient data in A Memory to fill B Memory (a trigger occurred before a full buffer of data was recorded), then B Memory will be padded with Don't Cares.
The B Memory may now be edited or used for Compare and Search operations.

C. Storing Data in Saved B Memory (See Figure 6.8a)

There must be data in the B Memory before executing a Save.
This data can be generated either by executing a copy A to B, a recall of a B Memory file, or a download of a B Memory.

To save B memory in nonvolatile storage, cursor to the Action field and depress the f1 key ("SAVE B"), then depress f1 again to verify the action. To recall a B Memory file, cursor to the Action field and depress the f2 key ("RECALL B"), then depress f2 again to verify the action. The current B Memory will be overwritten by the B Memory file selected.

As with the Set-up Storage screen, an asterisk to the left of the file number indicates the current B Memory file in use (last file accessed). An "M" to the right of the file number indicates that B Memory currently in the PM 36.8 differs from the file indicated by the asterisk.

If the RS-232C Communication Card or the ROM Emulator Module has been installed in the PM 3632, then B Memory can also be uploaded and downloaded (e.g. by the PM 4202 recorder, a controller, etc.)

To upload or download B Memory, cursor to the Action column and depress the f3 key ("UPLOAD B") or the f4 key ("DOWNLOAD B"). The B Memory is uploaded or downloaded to B Memory rather than a B Memory file, so the location of the cursor in the Action column is unimportant. The B Memory may then be saved in a B Memory file, if desired.

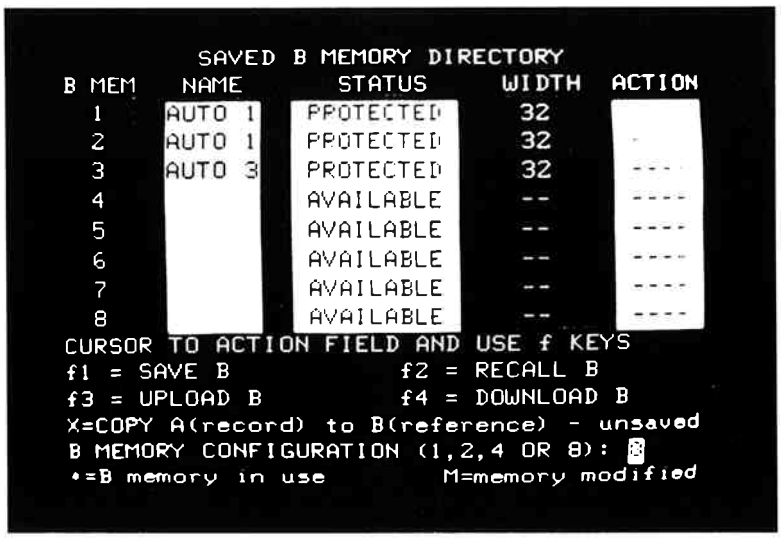


Fig. 6.8a *B Memory Screen (cursor in Action field)*

D. B Memory File Names (See Figure 6.8b)

B Memory files can be assigned names of up to six characters, before saving the file.

To enter a B Memory file name, cursor to each space in the Name field and enter one character at a time, using the f1 and f2 keys to alphabetically advance or retreat characters until the desired character is displayed in each space. The f3 key (clear field) may be used to clear the entire name field.

To change a B Memory file name, edit the name field one character at a time, using the f1 and f2 keys, then save the file again.
If a file name is changed without the file being resaved, a warning message will be issued if an attempt is made to exit the screen.

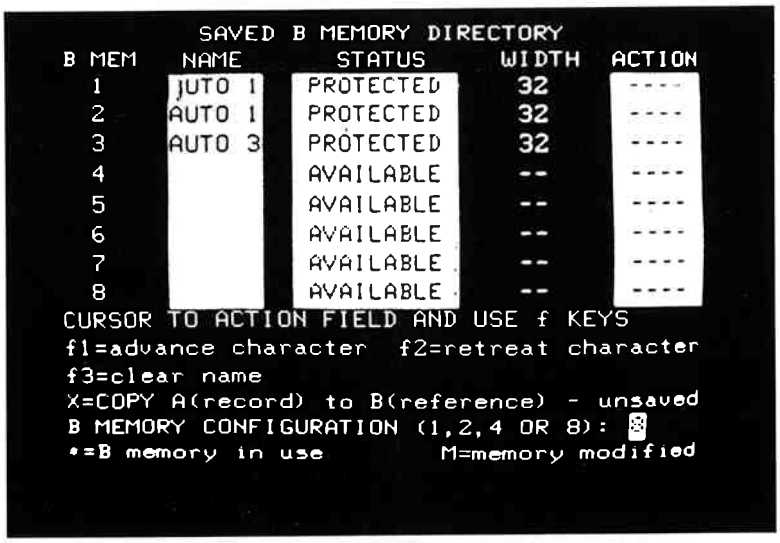


Fig. 6.8b *B Memory Screen (cursor in Name field)*

E. Status (Protected, Unprotected, Available) (See Figure 6.8c)

B Memory files normally have a status of "Unprotected," but may also be "Protected."

To protect a B Memory file, cursor to the Status field, depress the f3 key (protected), then save the file.
Before the file is saved, a security code will be requested; this is a 2-digit hexadecimal number which is entered via the keypad.
This code is not shown on the display (if more than two characters are entered only the last two apply).
The security code will be requested prior to any future attempt to write over the file.
It is strongly recommended that the security code be written down somewhere, and stored for future use.

To change a Protected file to Unprotected, cursor to the Status field, depress the f2 key (unprotected), and save the file again, using the correct security code.

To erase a B Memory file, cursor to the Status fiel, depress the f1 key (available), and save the file again.

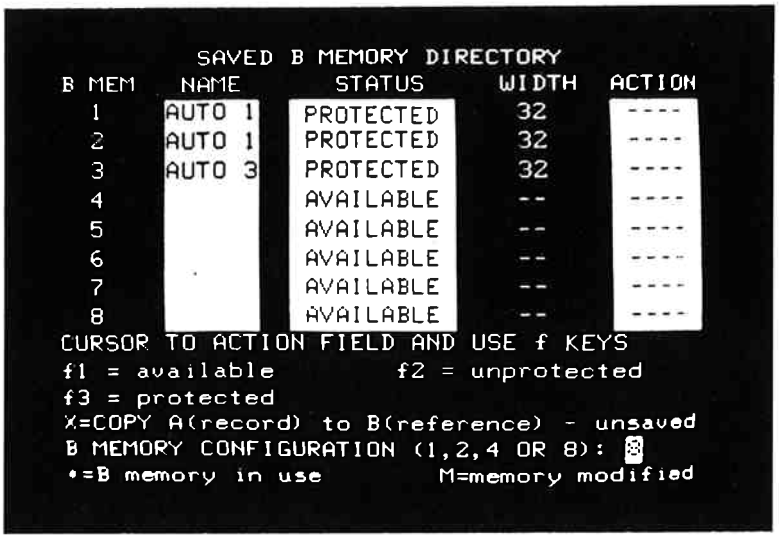


Fig. 6.8c *B Memory Screen (cursor in Status field)*

6.6.8 COMPARING DATA (With the PM 8880/50 only)
See Figures 6.9a--d.

A. General

The Compare screen is used to compare A (record) Memory to B (reference) Memory, using one of three methods:

* A Single Compare of already-captured data in A Memory to B Memory.

* A Continuous Compare where data is recaptured according to the machine set-ups, and compared to B Memory after each recapture.

* An Autosequencing Compare, which is similar to a Continuous Compare, except that up to 8 different machine set-ups and up to 8 different B memories (and thus up to 8 different Compare-functions) are performed a selected number of times.

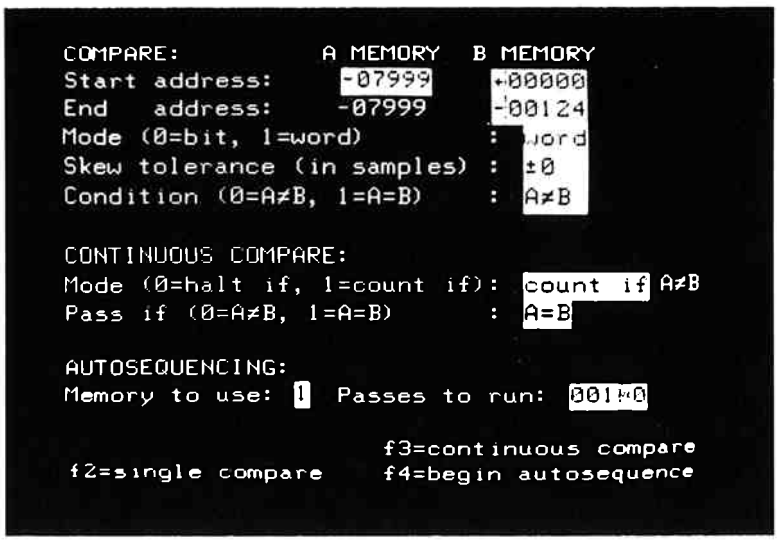


Fig. 6.9a *Compare Screen*

To execute any Compare, either depress the CLEAR key while in the Compare screen, or depress the START key to recapture data.
To abort a Compare, depress the STOP key.

Before comparing data, the user must select several comparison parameter:

* Data ranges for both A and B Memories by specifying:
  - The A Memory start address
  - The B Memory start address
  - The B Memory end address

* Comparison Mode (bit-to-bit or word-to-word)

* Skew Tolerance (jitter)

* Comparison Condition (A≠B or A=B)

Before performing a Single Compare, there must already be captured data in the A Memory and reference data in the B Memory.

The data in the B Memory may consist of:
- -Previously captured data that was copied to B Memory with the Copy command, or
- -a B Memory file that was recalled from the Saved B Memory Directory,
- -or data which was downloaded via the RS-232C interface.

To specify the data ranges for the A and the B Memories, cursor to the Address fields and enter the A Memory Start Address, the B Memory Start Address, and the B Memory End Address.
The two ranges of data to be compared are of the same size. The A Memory End address will be calculated and displayed automatically after the other three addresses are entered.

There are two modes of compare:
- Bit compare, in which words are compared on a bit-to-bit (channel-to-channel) basis, and
- Word compare, in which words are compared on a word-to-word basis.

To specify the comparison Mode, cursor to the Mode field and depress either 0 (bit basis) or 1 (word basis).

Bit or word compare

Bit compare is principally meant for compare functions of data recorded with the analyzer (=internal) clock, because sampled data depend strongly on the relations between the clock of the system under test and the analyzer clock.
With bit compare each sample is compared channel per channel. When skew (jitter) is allowed, bits in adjacent samples are included in the comparison, refer to next example.

Word compare is merely meant for compare functions of data recorded with the system (=external) clock. When skew is allowed the complete adjacent words will be included in comparison.

Skew

The maximum selectable amount of skew allowed is 9 samples (forwards and backwards). Skew allows the compare algorithm to be more flexible in comparing A to B Memories.

For example, microprocessor cycles sampled with the internal (asynchronuous) clock may appear a varying number of times in the buffer, depending upon how the internal clock and the microprocessor clock happened to line up at a given time. Allowing some skew in the Compare lets the Compare algorithm look up to skew words on either side of the word in reference memory to try to find a match.

The Skew value will directly affect the amount of time it takes to compare A and B Memories. As the value of allowable skew goes up, the number of checks that the machine must perform increases dramatically. For faster execution times, it is recommended that the Skew value, along with the range of addresses to compare, be kept no larger than is absolutely necessary.

To specify the Skew, put the cursor to the Skew Tolerance field and enter a value between 0 and 9.

Example

```
                    B Memory        A Memory

ch.0 -->            0001000         0100000
ch.1 -->            0001000         0001000
ch.2 -->            0001000         0000100
ch.3 -->            0001000         0100000
                       *
```

Compare results:

```
Word basis  :  Without skew       : Unequal
               With skew (+/- 3)  : Unequal

Bit basis   :  Without skew       : Unequal
               With skew (+/- 3)  : Equal
```

To specify the compare Condition, put the cursor to the Condition field and depress either 0 (to select A≠B) or 1 (to select A=B).

When it is desired to compare A and B Memories for differences, specify A≠B; for matches between A and B Memories, specify A=B. Occurrences of the differences or matches will be then be counted and high-lighted in the state display.

B. Single Compare

To execute a Single Compare (after specifying the above parameters), depress the f2 key (Single Compare). This will cause the screen to display the Compare Results, as shown in Figure 6.9b.

After a Single Compare, the number of occurrences of the compare condition, along with the address of the first and last occurrences, are displayed on the Compare screen (Figure 6.9b below). The occurrences of the compare condition are high-lighted in the STATE display.

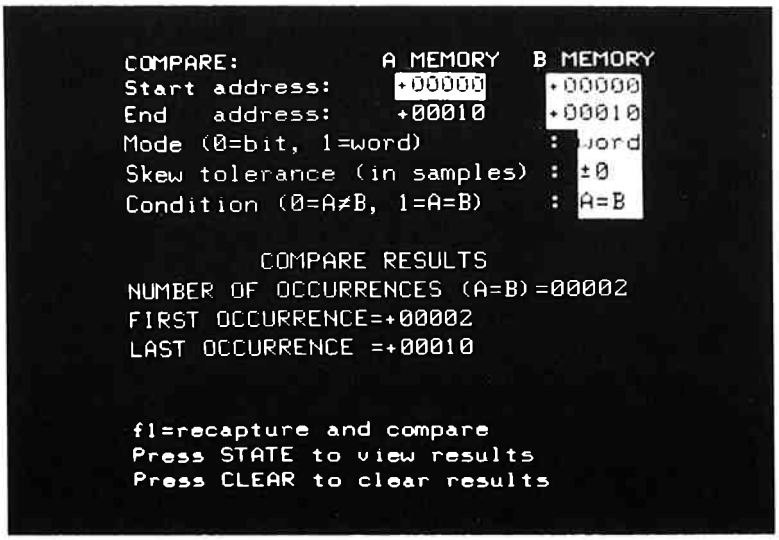


Fig. 6.9b *Compare Screen (Single Compare Results)*

To clear the results of a Compare, either depress the CLEAR key while in the Compare screen, or depress the START key to recapture data.
To recapture data and perform another Compare, depress the f1 key.
To abort a Compare, depress the STOP key.

It is often necessary to compare only selected fields in A and B Memories. This can be done by using B Memory edit to fill the fields to ignore with "Don't Cares", or by accessing the Format screen and turning off the fields to ignore.
Turning off fields does not destroy data in the B Memory. However, once parts of the B Memory has been edited to Don't Cares, there is no way to "un-Don't Care" the data; it must be saved and recalled from B Memory to restore the areas set to Don't Cares.

C. Continuous Compare

Continuous Compare is helpful in finding an intermittent bug that only seems to show itself when no one is expecting it.
Catching such a failure by performing Single Compares over and over again until it happens to be found is tedious; instead, the Continuous Compare feature can be used to direct the PM 3632 to do the looking itself, then either stop when it catches the failure or else count the number of times it sees it.

To perform a Continuous Compare, first specify the addresses, Compare mode, skew tolerance, and Compare condition as described in the Section 3.a above (Single Compare). Then specify the Continuous Compare mode (whether the PM 3632 should "Halt If" the condition is seen, or just "Count If" the condition is seen) and the pass condition (A≠B or A=B).
For example, if there is a known good "picture" in B Memory, then A=B would be a "Pass". Conversely, if a known bad picture has been seen (possibly a recurring fault found in production test), then A=B is a failure, and the pass condition would be A≠B.

To specify the Continuous Compare mode, cursor to the Continuous Compare Mode field and depress either the 0 key ("Halt If") or the 1 key ("Count If").
To specify the pass condition, depress either the 0 key (A≠B), or the 1 key (A=B).
To execute a Continuous Compare after specifying all of the necessary parameters, depress the f3 key. The results will be displayed, as shown in Figure 6.9c below.
To abort a Continuous Compare, depress the STOP key.

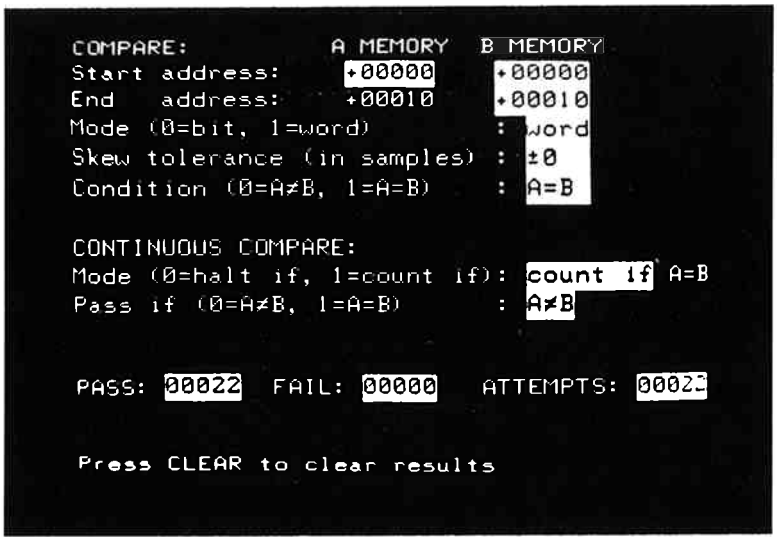


Fig. 6.9c *Compare Screen (Continuous Compare Results)*

The results of a Continuous Compare (number of passes, fails, and attempts) will be continuously displayed and updated on the Compare screen.
If the "Count If" Continuous Compare mode was specified, the compares will be executed forever, or until the STOP key is depressed.
If the "Half If" mode was specified, the compares will be performed only until the condition specified has been met or until the STOP key is depressed.

Compare that caused the halt, depress the CLEAR key once. As in a Single Compare, these results are high-lighted in the State display.
To clear the Compare results, depress the CLEAR key a second time.

Note that the Compare Condition to halt on and the condition specified as a failure (inverse of the Pass Condition) are two separate things; the The Compare does not halt on a failure, but halts when the Compare Condition is met.

The Pass, Fail, and Attempt counters roll over to zero at 65535.

D. Autosequencing (See Figures 6.9a and 6.9d)

Autosequencing was designed with production tests in mind.
It is a very powerful feature which allows at up to eight totally unrelated instrument settings, Compares to be made between captured data and saved reference data.

To perform autosequencing, specify:
-the parameters detailed in both Section 3.a (Single Compare) and Section 3.b (Continuous Compare), using the Compare screen.
-two more parameters (also using the Compare screen): (B) Memory To Use for compare (an already saved B Memory file) and the number of Passes To Run.

To specify the (B) Memory To Use, cursor to the Memory To Use field and enter the B Memory file number. To specify the number of Passes To Run, cursor to the Passes To Run field and enter the number (between 0 and 65535). See Figure 6.9a.

Next select the number of different Compares to perform by specifying the Autosequencing Start and End Files, using the Set-up Directory screen. For example, to run four different tests requiring capturing and comparing data at four different locations, set up the PM 3632 to trigger at the first location and capture data to use as a reference memeory. Then save this data in a B Memory file for later use, and also save the machine set-ups used to capture this data in a set-up file.

If the user has selected set-up file number 4 and file number 1 for the B Memory data, then this process should be repeated 3 more times, saving the set-up parameters used in set-up files 5, 6 and 7, and the B Memory pictures in B Memory files 2, 3 and 4. Then the selected Autosequencing Start File would be set-up file 4, and the End File would be set-up file 7.
Note that set-up files to use in Autosequencing must be in consecutive order; B Memories, however, may be in any order.

To execute Autosequencing, depress the f4 key while in the Compare screen. Autosequencing results will be displayed and updated continuously on the Autosequencing Results screen (Figure 6.9d); this screen is displayed automatically when an Autosequence is begun.
To abort Autosequencing, depress the STOP key.

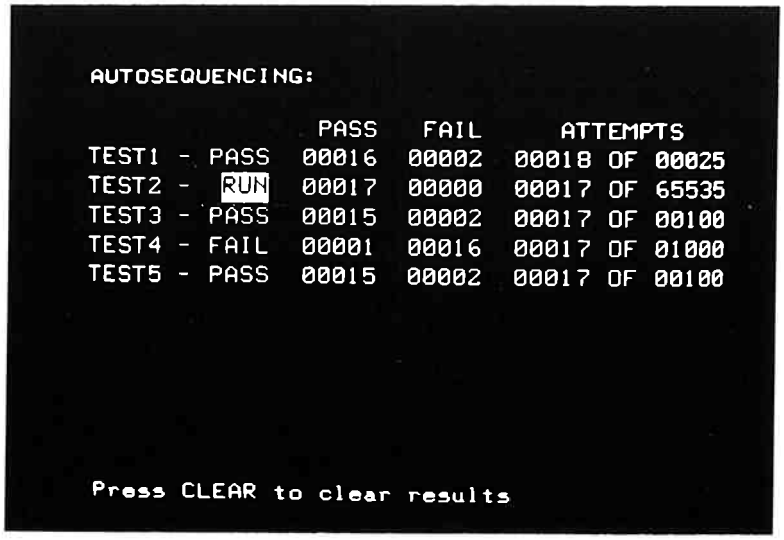


Fig. 6.9d *Autosequencing Results*

As Autosequencing begins, set-up file number 4 is read; it specifies the B Memory (file number 1) to load to use for the Compare.
Data is captured, the Compare is made, and the progress of Test 4 is updated.
Next, set-up file nuber 5 is read. It specifies a B Memory file (file number 2) of its own to use as reference data. The machine captures new data, performs a new Compare, and continues.
Each Autosequencing test runs until the Number of Passes to Run (specified in the Compare screen of each set-up file) has been executed.

Test numbers correspond to the set-up files in which the set-ups are stored. The number of passes, fails and attempts for each test is continuously updated, and the status of each test is displayed.

"RUN" means that the test is currently being run.
"PASS" means that the last time the test was run, it passed.
"FALL" means that the last time the test was run, it failed.
"DONE" means that the test has been run the number of passes requested and is now finished.
"HALT" means that Autosequencing has been halted because this test has encountered a "Halt If" condition.

To print a hard-copy record of the autosequencing results (only if the RS-232C Communications Card is installed) depress the f4 key.
There is no on-screen prompt for this print function of the f4 key.

6.6.9 SEARCH (PM 8880/50 only)

Press the S.FUNC key, then press key A.
The Search screen is used to search for a number of 1 to 10 words (labeled 0-9) in either A or B Memory.

A. Search word selection

To select the word(s) to be searched for, cursor to each of its fields and enter it via the numeric, X, and CLEAR keys on the keypad.

A search word can also be filled from a trigger word or from any Memory word.
To fill a search word with a trigger word, position the cursor in the word to fill, and depress f1 key (Set Word with Trigger); then select the trigger word to use (A, B, C, or D) and depress the f1 key to execute the fill.
To fill a search word with a memory word, first cursor to the Memory-to-Search field and select either A or B (the memory in which the word is located).
Next position the cursor in the word to be filled, and depress the f2 key. Then (using the cursor, numeric, f1 and CLEAR keys) enter the memory address location number, and execute the fill by depressing f2.

B. Which memory to search?

To specify which Memory to search, cursor to the Memory to Search field and enter A or B.

C. Search pattern

To define the pattern to search for, cursor to the Search Sequence fields and enter the numbers of the first and the last words which define the pattern to search for.
To search for a single word, enter the same number for both the first and last word.

D. Search execute

To execute the Search, depress the f3 key.
As soon as a Search has been executed, the Search results will be displayed on the Search screen.
For example, Figure 6.10 shows the results of a Search in the A Memory for and input from Port 0 (opcode fetch of a DB followed by a memory read of a 00). The number of search matches found, along with the addresses of the first and last matches, are shown on the screen. To view these matches high-lighted on the State display screen, depress STATE.

To clear the results of a Search, either depress CLEAR while in the Search screen, or depress START to capture new data.

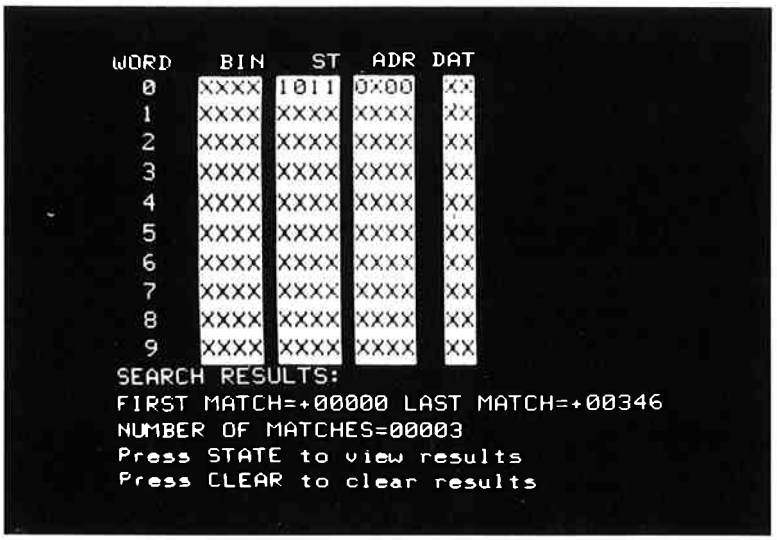


Fig. 6.10 *Search Screen (Results)*

6.6.10 B MEMORY EDIT (with PM 8080/50 only) (See Figure 6.11)

A. General

With this screen, the user can edit reference data in the B Memory. A typical use might be to enter Xs (Don't Cares) in some positions in the some fields so that a compare will ignore extraneous data.
As with all PM 3632 data displays, the user can direct the cursor to any desired address in the memory via the f1 key, and the cursor speed can be changed via the f2 key.

To edit B Memory data, use the f1 key and the Up and Down arrow keys to position the word to edit in the high-lighted edit window. Use the numeric, X, left and right cursor and CLEAR keys to edit the data to the desired value.

A range of addresses may be filled with a particular word or portion of a word. To fill a range of addresses with one identical word:
- First position one address of the range to fill (either Start or End Address), in the edit window, and depress the f3 key.
- Edit the data to the desired word to fill with.
- Position the other address of the fill range in the edit window, using the Up and Down arrows or the f1 key.
- Depress the f3 key to execute the fill.

To fill a range of addresses with a portion of a word.
- Depress the FORMAT key and change the display format to selectively turn off the fields that are to be left undisturbed by the fill.
- Execute the fill as described above, then return to the Format screen and turn all fields back on again.

NOTE: One disadvantage of this method is that portions of the trigger words are reset to Don't Cares; this problem can be alleviated by recalling a set-up file to restore the original trigger words.

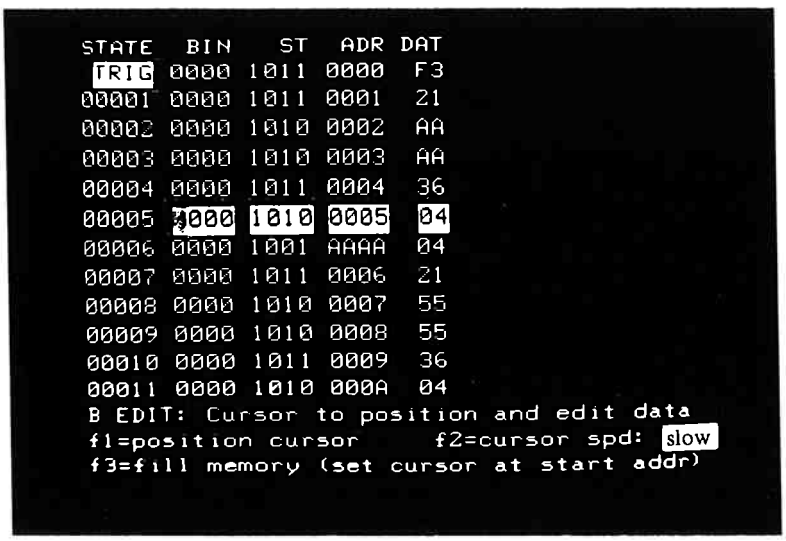


Fig. 6.11 *B Memory Edit Screen*

B. B Memory Display

B Memory is displayed only on the State screen.

A high-lighted A or B at the bottom of the State display screen indicates which Memory is being displayed. To display screen and depress either A or B to select the Memory to be displayed.

As with the A Memory, a pointer indicates the last displayed location in B Memory. When the State display screen is exited and re-entered, this pointer "remembers" the last area of Memory displayed.
In addition, as the cursor is moved through one memory, the pointer to the other Memory not being displayed is moved at the same time. If a corresponding address does not exist in the other Memory, the pointer is left undisturbed.

To print a hard-copy record of any portion of A or B Memory (if the RS-232C Communications card is present), depress the f4 key while viewing the State display screen. There is no on-screen prompt for this print function of the f4 key.

6.6.11 A and B MEMORY EXECUTION TIMES

A. Set-up Storage times

The time required to save a analyzer set-up file is directly proportional to the difference, in number of bytes, between the current analyzer set-ups and the old file to write over. This time is max. 2.5 seconds, but on the average isless than 1 second.

B. B Memory Storage times

The time required to save a B Memory file (data file) is directly proportional to the difference, in number of bytes, between the current B Memory and the old B Memory file to write over. In addition, the number of bytes in B Memory varies according to the B Memory configuration.

Storage times are:

B Memory files	Max. Storage Time
1	20.0 seconds
2	10.0 seconds
4	5.0 seconds
8	2.5 seconds

C. Copy A to B execution times

The time required to copy data in the A Memory to the B Memory is directly proportional to the number of samples to copy. The number of samples is dictated by the width of the machine.

Width	Approx. Copy Time
4	15.0 seconds
8	7.5 seconds
16	4.3 seconds
32	2.6 seconds

D. Search execution times

The time required to search a memory depends on the number of words to search (width of machine), the size of the memory (B Memory only) and, to a lesser degree, the number of matches found and the size of the search pattern.

The A Memory:

Width	Approx. Search Time
4	16.0 seconds
8	8.0 seconds
16	4.0 seconds
32	2.0 seconds

The B Memory:

Approx. Search Time (in sec.)

	Configuration			
Width	1	2	3	4
4	5.0	2.5	1.3	0.6
8	2.5	1.3	0.6	0.3
16	1.3	0.6	0.3	0.2
32	0.8	0.4	0.2	0.1

E. Compare execution times

The time required to compare the A Memory eith B Memory is dependent upon the size of the Compare range, the allowable skew in the Compare, and, to a lesser degree, the Compare mode (word- or bit basis) and the number of Compare occurrences found. Note also that, in continuous of Autosequencing compares, the machine may not need to compare the entire memories if "Count If" is selected. Sample Compare times are:

Approx. 3.5 seconds for:
- 32 bits wide
- Word compare
- 0 skew
- 1000 samples
- No occurences found

Approx. 135 seconds for: (Worst case)
- 4 bits wide
- Bit compare
- +/- 9 skew
- 8000 samples
- No occurences found

To keep Compare execution times to a minimum, keep the size of the Compare range and the allowable skew only as large as necessary. This is especially important in Continuous and Autosequencing compares, since the Compare time represents "dead" time regarding catching a failure. A typical compare of microprocessor data needs a Compare range of 100 samples and 0 skew; this Compare would take less than 1 second.

7 INSTALLATION INSTRUCTIONS

7.1 PREPARATIONS FOR USE

WARNING Remove the mains supply before:

-removing the instrument covers, or

-replacement of the mains fuse

to avoid any possibility of electrical shocks.

Mains Voltage

The PM 3632 as it is, has been provided for two mains voltages:
220 V and 240 V.

Setting for the mains voltage is done with two Faston colored-wire connections, located near the power supply transformer in the instrument.

220V

White/brown --><-- Blue(2x)

White/orange --><-- White(2x)

240V

White/brown --><-- White(2x)

White/orange --><-- Blue(2x)

(the white wires are non-connected dummy wires)

If required the PM 3632 can be adopted for the voltages 100, 110, 120, 127, 200 or 250 V. For this we recommend you to contact your local Philips Service Center.

Mains fuse

The value of the mains fuse is depending on the mains voltage:
110...127V : 2 Amps (delayed)
200...250V : 1 Amp (delayed)
5x20mm, glass tube.

This fuse is located in the rear panel of the instrument.

Mains frequency, 50 or 60 Hz

With instruments with serial nr 1850 and higher, the mains frequency adaptation is not selectable by the user.
Please contact your local Philips Service Center.

7.2 BUILDING-IN THE OPTIONS

Inside the PM 3632 on the main p.c.board there are three slots to accomodate the option boards.

7.2.1 General Procedure

-Disconnect the mains voltage.
-Remove both the front panel- and the rear panel rims (eight screws).
-Lift the top cabinet plate.
-Remove the retainer bracket which is mounted over the main p.c. board in
-Mount the bracket to secure the option unit(s).
-Fix the top cabinet plate.
-Fix both the front panel- and the rear panel rims.

7.2.2 RS-232C Communication Card PM 8880/20

This card which is used with Data-Transfer and with Rom-Emulation, is not field-installable.
Also the PM 8880/00, which consists of the Rom Emulator Pod and the RS-232C Communication card is not field-installable.
For building-in this option contact your local Philips Service Shop.
All RS-232C Port configuration settings are controlled via the specific menu.
For RS-232C cable connections refer to chapter 6.2.

7.2.3 Disassembly Rom board PM 8880/30

Mount this unit in the right-hand side slot on the main p.c. board.
For each specific Microprocessor Pod the corresponding Disassembly Prom must be located on this unit.

Disa Prom
Included with each Microprocessor Pod (8- or 16 bit) is a Prom, used for disassembly.
These Proms must be installed on the Disassembly Rom board (PM 8880/30).

16-Bit Microprocessors Trigger Prom
This Prom (labelled "MT600-*") must be installed on the Disassembly Rom board, when a 16-bit microprocessor pod has been connected.

Prom location
Proms type 2732 and type 2764 may be located in any socket (U1--8) on this board.
Proms type 27128 may only be located in sockets U5--8.

Refer to Figure 7.1 on next page.

7.2.4 Set-up/and Data memory board PM 8880/40/50

Mount this unit in the centre slot on the main p.c. board.

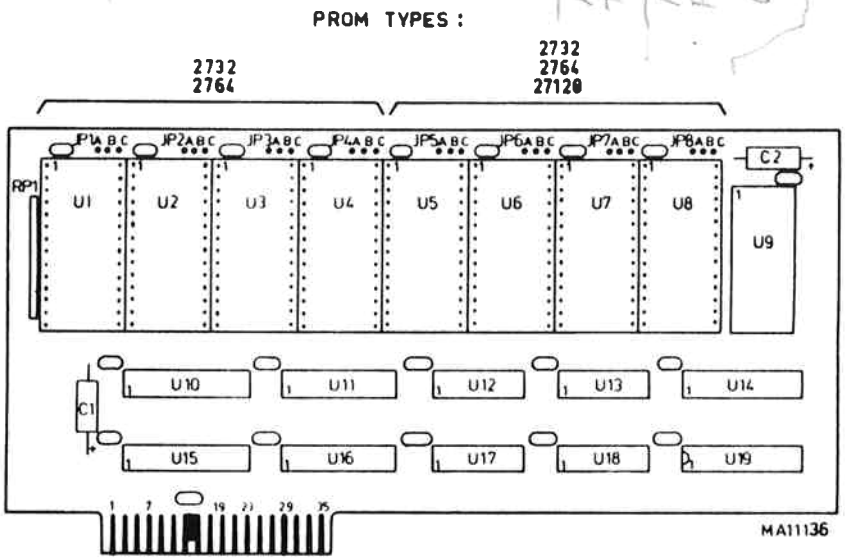


Fig. 7.1 *Location of the various types of Proms on the Disassembly Rom Board.*

7.3 PROM OVERVIEW

The following proms may be present in the PM 3632.

Label	Description
M4P00-*	These two proms are the basic PM 3632
M4P01-*	system software.
M4F00-*	Same as M4P00-* and M4P01-*, but with
M4F01-*	French screen text.
MCH01-*	Character generator
MSM00-*	Setup memory
MA800-*	Setup and Data memory
MRE00-*	RS-232C Rom Emulation unit
→ MIN00-*	Disassembly Prom for PM 8865 microprocessor pod
M6800-*	Disassembly Prom for PM 8866 microprocessor pod
M6900-*	Disassembly Prom for PM 8867 microprocessor pod
M6500-*	Disassembly Prom for PM 8868 microprocessor pod
MZ800-*	Disassembly Prom for PM 8869 microprocessor pod
M8N00-*	Disassembly Prom for PM 8870 microprocessor pod
→ MT600-*	Trigger Prom required for 16-bit-microprocessors pods
→ M6K00-*	Disassembly Prom for PM 8874 microprocessor pod (68000/68010)
M8600-*	Disassembly Prom for PM 8876 microprocessor pod (8086/8088)

* = a letter indicating the software release.

APPENDIX 1

DISPLAY MESSAGES

-1 OR 2 WORDS ONLY (Configuration)	In state qualification only two words are allowed for each entry.
-ACCESS DENIED (Setup Directory and B Memory Directory)	The wrong security code was entered while trying to read a protected setup- or B Memory file.
-ADDRESS NOT FOUND (Search and Compare)	One of the 3 addresses specified in a Compare was not found in either A or B Memory, or the address specified in Fill with Memory (Search) was not found.
-ACTIVE	Data recording is running.
-ALREADY STARTED (any)	The START key was depressed when the PM 3632 was already active.
-A/B RAM FAILURE	Probably memory-circuit failure on PM 8880/50 option board.
-CANNOT WRITE OVER PROTECTED FILES (B Memory Directory)	An attempt was made to write a B Memory file, with a new configuration differing from the stored configuration, over a protected file. The protected file must be unprotected first.
-CAN'T DISASSEMBLE--CS READS USED AS OPCODES (8086/8088 Disa)	Correct disassembly not possible. Refer to page 5-53.
-CAN'T DISASSEMBLE--PS READS USED AS OPCODES (68000/68010 Disa)	Correct disassembly not possible. Refer to page 5-34.
-CHECKSUM ERROR - FILE LOST (Setup Directory, B Memory Directory and Status)	A checksum error occurred while reading a setup- or B Memory file. This indicates a hardware problem on the PM 8880/40/50 unit.
-COMPARE RANGES UNEQUAL (Compare)	Compare ranges do not correspond.

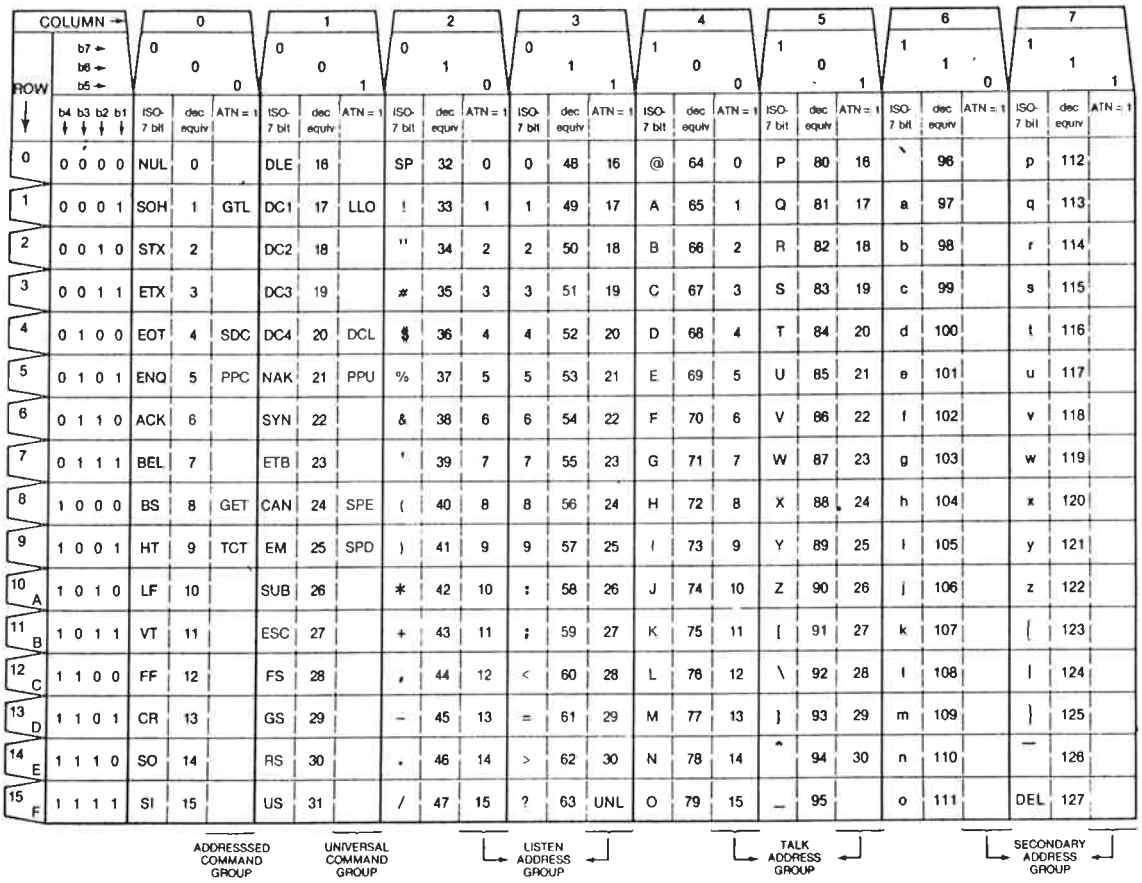
-DIRECTORY CHECKSUM ERROR- ALL FILES LOST (Setup Directory, B Memory Directory and Status)	A checksum error occurred while reading the EEPROM directory information. This indicates a hardware problem on the PM 8880/40/50 unit.
-FILE CONFLICTS WITH POD TYPE (Setup Directory)	An attempt was made to read a setup file with the wrong Pod connected to the PM 3632.
-FILE DOES NOT EXIST (Setup Directory and B Memory Directory)	An attempt was made to read an available (non existent) setup- or B Memory file.
-FILE NO. INCONSISTENT WITH CONFIGURATION (B Memory Directory)	An attempt was made to save a B Memory file in a file number larger than the new B Memory configuration. This can occur only when changing to a smaller B configuration.
-FILE WIDTH DIFFERS FROM MACHINE WIDTH (B Memory Directory)	An attempt was made to read a B Memory file stored with a width differing from the current width of the PM 3632.
-FORMAT INCONSISTENT WITH WIDTH (Timing and State)	"Probe" numbers higher than those used in the selected configuration have been used in the display format (see FORMAT screen).
-ILLEGAL COMBINATION (Status)	The two flashing parameters may not be set to their current values at the same time.
-IMPROPER FILE ORDER FOR AUTOSEQUENCING (Setup Directory)	An attempt was made to exit the Setup Directory screen with the Auto-sequencing start file number larger than the autosequencing end file number.
-INCORRECT SEARCH SEQUENCE (Search)	An attempt was made to execute a Search with the first search word after the last search word.
-LOW PROBE MUST BE LESS THAN HIGH PROBE (Format)	When defining display fields via the Format screen, the "Low Probe" must have a lower probe number than the "High Probe".
-MEMORY CONFIGURATION INCONSISTENT (B Memory Directory)	An attempt was made to read a B Memory file stored under a configuration differing from the current B Memory configuration.

-MUST NOT EXCEED 13 (Trigger sequence)	The total number of trigger delay in events may not be more than 13.
-NO DATA IN B MEMORY (B Memory Directory, Search, Compare, Edit and State)	An attempt was made to save, edit, display, search or upload B Memory while B Memory is empty.
-NO DATA RECORDED (any)	The START and STOP keys were depressed but less than two qualified samples occurred after starting but before stopping.
-NO FIELDS TO EDIT (Edit)	An attempt was made to edit B Memory with all fields in the Format screen turned off.
-NO RECORDED DATA (B Memory Directory and State)	An attempt was made to copy A Memory to B Memory when A Memory was empty, or a display key was pressed to view A Memory when it was empty.
-NOT ACTIVE (any)	The STOP key was depressed when the PM 3632 was not active.
-POD CONNECTION ERROR (any)	The connection from the Pod to the circuit under test is either not made or made incorrectly, or the microprocessor is not powered (microprocessor Pods). With the 8086/8088 microprocessor pod switch 1 not corresponding with the target mode. Refer to page 5-42.
-POD x ROM x NOT USED BUT INSTALLED (when exiting the Rom Emulator Editor)	The specified DIP-cable is installed in a Rom socket, but is not defined on the "Rom Emulator Configuration" screen.
-POD x ROM x INSTALLATION ERROR (When exiting the Rom Emulator Editor)	The specified DIP-cable is not installed correctly in a powered Rom socket, but is defined on the Rom Emulator Configuration Screen.
-SELECTED FORMAT TOO WIDE FOR SCREEN (Format)	If a display was created from the keyed-in parameters, one or more of the fields would extent off the right side of the screen.
-START ADDR > END ADDR (Compare)	An attempt was made to execute a Compare with the starting address in memory higher than the ending address.

-TRIGGER TOO COMPLEX (16-bit microproc. pods)	The selected trigger sequence will not work. Refer to page 5-27 for 68000/68010, or page 5-46 for 8086/8088.
-UNABLE TO DISASSEMBLE XXX CYCLES (16-bit microproc. pods)	A number of cycles cannot be disassembled. Refer to page 5-34 for 68000/68010, or page 5-53 for 8086/8088.
-WARNING-UNSAVED NAME & STATUS WILL BE LOST (Setup Directory and B Memory Directory)	An attempt was made to leave the Setup Directory screen or the B Memory Directory screen without saving a file after changing its name and/or status.

APPENDIX 2

ASCII



ROW	b4 b3 b2 b1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
		ISO-7 bit / dec equiv / ATN=1	ISO-7 bit / dec equiv / ATN=1	ISO-7 bit / dec equiv / ATN=1	ISO-7 bit / dec equiv / ATN=1	ISO-7 bit / dec equiv / ATN=1	ISO-7 bit / dec equiv / ATN=1	ISO-7 bit / dec equiv / ATN=1	ISO-7 bit / dec equiv / ATN=1
0	0 0 0 0	NUL 0	DLE 16	SP 32 0	0 48 16	@ 64 0	P 80 16	` 96	p 112
1	0 0 0 1	SOH 1 GTL	DC1 17 LLO	! 33 1	1 49 17	A 65 1	Q 81 17	a 97	q 113
2	0 0 1 0	STX 2	DC2 18	" 34 2	2 50 18	B 66 2	R 82 18	b 98	r 114
3	0 0 1 1	ETX 3	DC3 19	# 35 3	3 51 19	C 67 3	S 83 19	c 99	s 115
4	0 1 0 0	EOT 4 SDC	DC4 20 DCL	$ 36 4	4 52 20	D 68 4	T 84 20	d 100	t 116
5	0 1 0 1	ENQ 5 PPC	NAK 21 PPU	% 37 5	5 53 21	E 69 5	U 85 21	e 101	u 117
6	0 1 1 0	ACK 6	SYN 22	& 38 6	6 54 22	F 70 6	V 86 22	f 102	v 118
7	0 1 1 1	BEL 7	ETB 23	' 39 7	7 55 23	G 71 7	W 87 23	g 103	w 119
8	1 0 0 0	BS 8 GET	CAN 24 SPE	(40 8	8 56 24	H 72 8	X 88 24	h 104	x 120
9	1 0 0 1	HT 9 TCT	EM 25 SPD	) 41 9	9 57 25	I 73 9	Y 89 25	i 105	y 121
10 A	1 0 1 0	LF 10	SUB 26	* 42 10	: 58 26	J 74 10	Z 90 26	j 106	z 122
11 B	1 0 1 1	VT 11	ESC 27	+ 43 11	; 59 27	K 75 11	[91 27	k 107	{ 123
12 C	1 1 0 0	FF 12	FS 28	, 44 12	< 60 28	L 76 12	\ 92 28	l 108	| 124
13 D	1 1 0 1	CR 13	GS 29	- 45 13	= 61 29	M 77 13	] 93 29	m 109	} 125
14 E	1 1 1 0	SO 14	RS 30	. 46 14	> 62 30	N 78 14	^ 94 30	n 110	~ 126
15 F	1 1 1 1	SI 15	US 31	/ 47 15	? 63 UNL	O 79 15	_ 95	o 111	DEL 127

ADDRESSSED COMMAND GROUP · UNIVERSAL COMMAND GROUP · LISTEN ADDRESS GROUP · TALK ADDRESS GROUP · SECONDARY ADDRESS GROUP

NUL	Null, or all zeroes	DC1	Device control 1
SOH	Start of heading	DC2	Device control 2
STX	Start of text	DC3	Device control 3
ETX	End of text	DC4	Device control 4
EOT	End of transmission	NAK	Negative acknowledge
ENQ	Enquiry	SYN	Synchronous idle
ACK	Acknowledge	ETB	End of transmissionblock
BEL	Bell, or alarm	CAN	Cancel
BS	Backspace	EM	End of medium
HT	Horizontal tabulation	SUB	Substitute
LF	Line feed	ESC	Escape
VT	Vertical tabulation	FS	File separator
FF	Form feed	GS	Group separator
CR	Carriage return	RS	Record separator
SO	Shift out	US	Unit separator
SI	Shift in	SP	Space
DLE	Data link escape	DEL	Delete

APPENDIX 3

INTEL HEX FORMAT

Intel Hex is an Intel Corporation format which provides a means of storing and transmitting object code. It is composed of variable length records which contain 7-bit ASCII codes.
By convention, usually only long, continuously defined memory images are transmitted, in 16-byte increments and beginning with adresses which are a multiple of 16.

In the actual record, all values are bytes or multiple bytes, and each byte is represented by two ASCII characters (0-9 or A-F). This includes byte count, load adress, record type, checksum and data.

The format is:

:BCAAAATTHhHhHhHhHhHhHhHhCC

where:

: (the ASCII character colon) is the start of the record.

BC is two ASCII characters which represent the hex value of the byte count (total number of data bytes)

AAAA is four characters representing two bytes of address (most significant byte first);

TT is two ASCII characters which represent the hex value of the record type:
- 00 = a data record.
- 01 = an end-of-file record.
- 02 = an extended address record for 16-bit microprocessors.

Hh is two ASCII characters which represent the hex value of a data byte.
There may be up to 256 data bytes, depending on the value of BC above and the device handlers in the equipment; normally, there are 16 or less.

CC is two ASCII characters which represent the hex value of the modulo 256 checksum of:
- Record length bytes (BC)
- Record type bytes (TT)
- All data bytes (Hh)

Records are terminated with a carriage return and a line feed.
The last record is always an end record.

As an example, the following program section (five bytes) would be tranfered as shown below it:

```
00 00 C3 00 00
--------------
:03000000C300003A   (data record)
:00000001FF         (end record)
```

APPENDIX 4

B-MEMORY UPLOAD/DOWNLOAD FORMAT

The size of a B memory transfer depends on the current B memory configuration.
The number of bytes transferred, and their order is as follows:

Data bytes transferred	B memory configuration 1	2	4	8
1) B data memory	4000	2000	1000	500
2) B mask data memory	4000	2000	1000	500
3) B memory configuration	1	1	1	1
4) Width	1	1	1	1
5) Starting state line number	2	2	2	2
Total number of bytes transferred:	8004	4004	2004	1004

Data bytes with their addresses (hex):

	B memory configuration 1	2	4	8
1) B data memory	0000-0F9F	0000-07CF	0000-03E7	0000-01F3
2) B mask data memory	0FA0-1F3F	07D0-0F9F	03E8-07CF	01F4-03E7
3) B memory configuration	1F40	0FA0	07D0	04E8
4) Width	1F41	0FA1	07D1	04E9
5) Starting state line number	1F42-1F43	0FA2-0FA3	07D2-07D3	04EA-04EB

B memory format:

```
Width= 4
byte 0: b7--b4 = 1st sample in memory
        b3--b0 = 2nd sample in memory
byte 1: b7--b4 = 3rd sample in memory
 etc.

Width= 8
byte 0: b7--b0 = 1st sample in memory
byte 1: b7--b0 = 2nd sample in memory
 etc.

Width= 16
byte 0: b7--b0  of 1st sample in memory
byte 1: b15--b8 of 1st sample in memory
byte 2: b7--b0  of 2nd sample in memory
 etc.

Width= 32
byte 0: b7--b0   of 1st sample in memory
byte 1: b15--b8  of 1st sample in memory
byte 2: b23--b16 of 1st sample in memory
byte 3: b31--b24 of 1st sample in memory
byte 4: b7--b0   of 2nd sample in memory
 etc.
```

```
Width= 62
byte 0: b7--b0   of 1st sample in memory
byte 1: b15--b8  of 1st sample in memory
byte 2: b23--b16 of 1st sample in memory
byte 3: b31--b24 of 1st sample in memory
byte 4: b39--b32 of 1st sample in memory
byte 5: b47--b40 of 1st sample in memory
byte 6: b55--b48 of 1st sample in memory
byte 7: b63--b56 of 1st sample in memory
byte 8: b7--b0   of 2nd sample in memory
```

B Mask Data Memory:
The B mask data memory has a bit for bit correspondence with the B data memory.
If a mask bit is 0, the corresponding data bit is a don't care (x).

There are three reasons why a B data memory bit may be a don't care:
1) The bit corresponds to an inactive probe line.
2) The bit was edited to a don't care bit via the B memory edit screen.
3) When A memory was copied to B memory, the A memory wasn't completely full. In this case the B memory is padded with don't cares.

B Memory Configuration Byte:
This byte is set to 1, 2, 4 or 8 indicating the B memory configuration at upload time.
If the B memory configuration during download doesn't match this byte, an error message will occur.

Width:
A byte indicating the width of the recorded data of the Logic Analyzer at upload time, see following table.

b7	b6	b5	Width
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64 (16-bit microprocessor pods)

If the width during download doesn't match this byte, an error message will occur.

Starting State Line Number:
A 2 byte value (LSB first) indicating the first state line number in the B Memory.
The largest possible negative starting state line number is -7999 (E0C1H), this is with a machine width of 4, and a trigger delay of 0.
The largest possible positive starting state line number is 49001 (BF69H), this is with a machine width of 32, and a trigger delay of 50000.

If this value is <= BF69H the starting state line number is positive, and is the value.
If this value is > BF69H then the starting state line number is negative, and is the 2's complement of the value.

Examples:
  Value 0BB8H indicates starting state line number 3000.

  Value FFFFH:
              = 1111 1111 1111 1111,
  minus 1   = 1111 1111 1111 1110,
  complement = 0000 0000 0000 0001,
                    indicating the starting state line number being: -1.

ALPHABETICAL INDEX